SCXI-1163 User Manual

32-Channel Isolated Digital Output Module

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About This Manual

This manual describes the electrical and mechanical aspects of the SCXI-1163 and contains information concerning its operation and programming. The SCXI-1163 is a member of the National Instruments Signal Conditioning eXtensions for Instrumentation (SCXI) Series modules for the National Instruments data acquisition plug-in boards. This module provides 32 isolated digital outputs configured in ports of four channels. Each port is isolated from other ports and from the internal circuitry of the SCXI-1163.

This manual describes the installation, basic programming considerations, and theory of operation for the SCXI-1163.

Organization of This Manual

The SCXI-1163 User Manual is organized as follows:

- Chapter 1, *Introduction*, describes the SCXI-1163; lists the contents of your SCXI-1163 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1163 kit.
- Chapter 2, *Configuration and Installation*, describes the SCXI-1163 jumper configurations, installation of the SCXI-1163 into the SCXI chassis, signal connections to the SCXI-1163, and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the SCXI-1163 module and explains the operation of each functional unit making up the SCXI-1163.
- Chapter 4, *Register Descriptions*, describes in detail the SCXI-1163 Address Handler, the Module ID Register, the Data Register, the Status registers, and the SCXI-1000/1001 Slot 0 registers.
- Chapter 5, *Programming*, contains a functional programming description of the SCXI-1163 and Slot 0.
- Appendix A, *Specifications*, lists the specifications for the SCXI-1163.
- Appendix B, *Rear Signal Connector*, describes the pinout and signal names for the SCXI-1163 50-pin rear signal connector, including a description of each connection.
- Appendix C, *SCXIbus Connector*, describes the pinout and signal names for the SCXI-1163 SCXIbus connector, including a description of each connection.
- Appendix D, *SCXI-1163 Front Connector*, describes the pinout and signal names for the SCXI-1163 front connector, including a description of each connection.
- Appendix E, *SCXI-1163 Cabling*, describes how to use and install the hardware accessories for the SCXI-1163.
- Appendix F, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.

- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

DIO board DIO board refers to the National Instruments AT-DIO-32F, MC-DIO-24,

MC-DIO-32F, NB-DIO-24, NB-DIO-32F, NB-DIO-96, PC-DIO-24, and PC-DIO-96 digital I/O data acquisition boards unless otherwise noted.

DIO-type board DIO-type board refers to National Instruments data acquisition boards that

have only digital inputs and outputs. These boards include the DIO-24,

DIO-32F, and DIO-96 boards unless otherwise noted.

italic Italic text denotes emphasis, a cross reference, or an introduction to a key

concept.

Lab board Lab board refers to the National Instruments Lab-LC, Lab-NB, Lab-PC,

and Lab-PC+ boards unless otherwise noted.

MC MC refers to the Micro Channel series computers.

MIO board MIO board refers to the National Instruments AT-MIO-16, AT-MIO-16D,

AT-MIO-16F-5, AT-MIO-16X, AT-MIO-64F-5, MC-MIO-16,

NB-MIO-16, and NB-MIO-16X multichannel I/O data acquisition boards

unless otherwise noted.

MIO-type board MIO-type board refers to National Instruments data acquisition boards that

have at least analog and digital inputs and outputs. These boards include the MIO boards, the Lab boards, and the PC-LPM-16 board unless

otherwise noted.

monospace Lowercase text in this font denotes text or characters that are to be literally

input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements

and comments taken from program code.

NB NB refers to the NuBus series computers.

PC PC refers to the IBM PC/XT, the IBM PC AT, and compatible computers.

SCXIbus SCXIbus refers to the backplane in the chassis. A signal on the backplane

is referred to as the SCXIbus < signal name > line (or signal).

The SCXIbus descriptor may be omitted when the meaning is clear. Descriptions of all SCXIbus signals are given in Appendix C, SCXIbus

Connector.

Slot 0 Slot 0 refers to the power supply and control circuitry in the SCXI chassis.

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- *AT-DIO-32F User Manual* (part number 320147-01)
- AT-MIO-16 User Manual (part number 320476-01)
- AT-MIO-16D User Manual (part number 320489-01)
- *AT-MIO-16F-5 User Manual* (part number 320266-01)
- AT-MIO-16X User Manual (part number 320488-01)
- AT-MIO-64F-5 User Manual (part number 320487-01)
- Lab-LC User Manual (part number 320380-01)
- Lab-NB User Manual (part number 320174-01)
- Lab-PC User Manual (part number 320205-01)
- Lab-PC+ User Manual (part number 320502-01)
- MC-DIO-24 User Manual (part number 320129-01)
- MC-DIO-32F User Manual (part number 320128-01)
- *MC-MIO-16 User Manual*, Revisions A to C (part number 320130-01)
- MC-MIO-16 User Manual, Revision D (part number 320560-01)
- NB-DIO-24 User Manual (part number 320094-01)
- NB-DIO-32F User Manual (part number 320095-01)
- NB-DIO-96 User Manual (part number 320384-01)
- NB-MIO-16 User Manual (part number 320295-01)
- NB-MIO-16X User Manual (part number 320157-01)
- *PC-DIO-24 User Manual* (part number 320288-01)
- *PC-DIO-96 User Manual* (part number 320289-01)
- *PC-LPM-16 User Manual* (part number 320287-01)
- *SCXI-1000/1001 User Manual* (part number 320423-01)

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix F, *Customer Communication*, at the end of this manual.

Chapter 1 Introduction

This chapter describes the SCXI-1163; lists the contents of your SCXI-1163 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1163 kit.

Figure 1-1 shows the SCXI-1163 module.

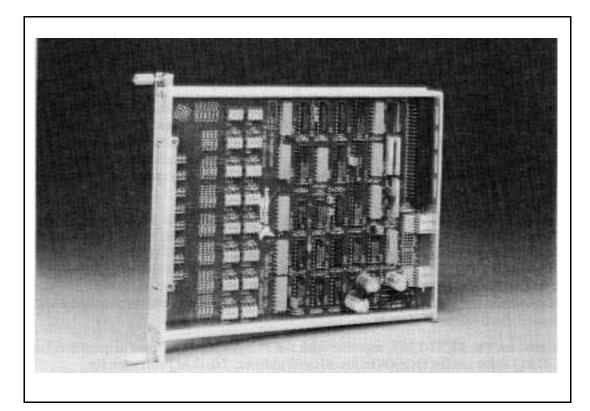


Figure 1-1. SCXI-1163 Digital Output Module

The SCXI-1163 is an SCXI module consisting of 32 optically isolated digital outputs. The SCXI-1163 module provides digital signals where common-mode voltages may be present.

The SCXI-1163 operates with full functionality with National Instruments MIO boards; Lab-NB, Lab-PC, Lab-PC+, Lab-LC, and PC-LPM-16 boards; and with the DIO-24, DIO-32F, and DIO-96 boards. You can also use the SCXI-1163 with other systems that comply with the specifications given in Chapter 2, *Configuration and Installation*. You can control several SCXI-1163s in a single chassis with one data acquisition board.

An additional shielded terminal block, the SCXI-1326, has screw terminals for easy signal attachment to the SCXI-1163.

Introduction Chapter 1

With the SCXI-1163, you can use the SCXI chassis as a controller in laboratory testing, production testing, and industrial-process monitoring.

What You Need To Get Started

| SCXI-1163 module |
|-----------------------|
| SCXI-1163 User Manual |
| SCXI chassis |
| Your computer |

Optional Software

This manual contains complete instructions for directly programming the SCXI-1163. You can order separate software packages for controlling the SCXI-1163 from National Instruments.

When you combine the PC, AT, and MC data acquisition boards with the SCXI-1163, you can use LabVIEW for Windows or LabWindows for DOS. LabVIEW and LabWindows are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances Microsoft C and QuickBASIC. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

Your National Instruments data acquisition board is shipped with the NI-DAQ software. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code.

You can also use the SCXI-1163, together with the PC, AT, and MC data acquisition boards, with NI-DAQ software for DOS/Windows/LabWindows. NI-DAQ software for DOS/Windows/LabWindows comes with language interfaces for Professional BASIC, Turbo Pascal, Turbo C, Turbo C++, Borland C++, and Microsoft C for DOS; and Visual Basic, Turbo Pascal, Microsoft C with SDK, and Borland C++ for Windows. NI-DAQ software for DOS/Windows/LabWindows is on high-density 5.25 in. and 3.5 in. diskettes.

You can use the SCXI-1163, together with the NB Series data acquisition boards, with LabVIEW for Macintosh, a software system that features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments boards, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software for Macintosh.

Chapter 1 Introduction

You can also use the SCXI-1163, combined with the NB Series data acquisition boards, with NI-DAQ software for Macintosh. NI-DAQ software for Macintosh, which is shipped with all National Instruments Macintosh data acquisition boards, comes with language interfaces for MPW C, THINK C, Pascal, and Microsoft QuickBASIC. Any language that uses Device Manager Toolbox calls can access NI-DAQ software for Macintosh.

Optional Equipment

- SCXI-1326 front terminal block
- SCXI-1340 cable assembly
- SCXI-1341 Lab-NB/Lab-PC/Lab-PC+ cable assembly
- SCXI-1342 PC-LPM-16 cable assembly
- SCXI-1343 rear screw terminal adapter
- SCXI-1344 Lab-LC cable assembly
- SCXI-1348 DIO-32F cable assembly
- SCXI-1350 multichassis adapter
- SCXI-1351 one-slot cable extender
- Standard ribbon cable 0.5 m 1.0 m
 NB5 cable 0.5 m 1.0 m

Refer to the *Signal Connections* section in Chapter 2, *Configuration and Installation*, and to Appendix E, *SCXI-1163 Cabling*, for additional information on cabling, connectors, and adapters.

Custom Cables

The SCXI-1163 rear signal connector is a 50-pin male ribbon-cable header. The manufacturer part number National Instruments uses for this header is as follows:

• AMP Inc. (part number 1-103310-0)

The mating connector for the SCXI-1163 rear signal connector is a 50-position polarized ribbon-socket connector with strain relief. National Instruments uses a polarized or keyed connector to prevent inadvertent upside-down connection to the SCXI-1163. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

Standard 50-conductor 28 AWG stranded ribbon cables that work with these connectors are as follows:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

The SCXI-1163 front connector is a special 48-pin DIN C male connector. The manufacturer part number National Instruments uses for this connector is as follows:

Introduction Chapter 1

• ERNI Components, Inc. (part number 033-273)

The mating connector for the SCXI-1163 front connector is a special 48-pin reversed DIN C female connector. National Instruments uses a polarized and keyed connector to prevent inadvertent upside-down connection to the SCXI-1163. The manufacturer part number National Instruments uses for this mating connector is as follows:

• ERNI Components, Inc. (part number 913-495)

National Instruments selected these connectors to meet UL 1244 for 450 Vrms working isolation.

Unpacking

Your SCXI-1163 module is shipped in an antistatic package to prevent electrostatic damage to the module. Several components on the module can be damaged by electrostatic discharge. To avoid such damage in handling the module, take the following precautions:

- Touch the antistatic package to a metal part of your SCXI chassis before removing the module from the package.
- Remove the module from the package and inspect the module for loose components or any other sign of damage. Notify National Instruments if the module appears damaged in any way. *Do not* install a damaged module into your SCXI chassis.

Chapter 2 Configuration and Installation

This chapter describes the SCXI-1163 jumper configurations, installation of the SCXI-1163 into the SCXI chassis, signal connections to the SCXI-1163, and cable wiring.

Module Configuration

The SCXI-1163 module consists of five user-configurable jumpers and one reserved jumper as shown in the parts locator diagram, Figure 2-1.

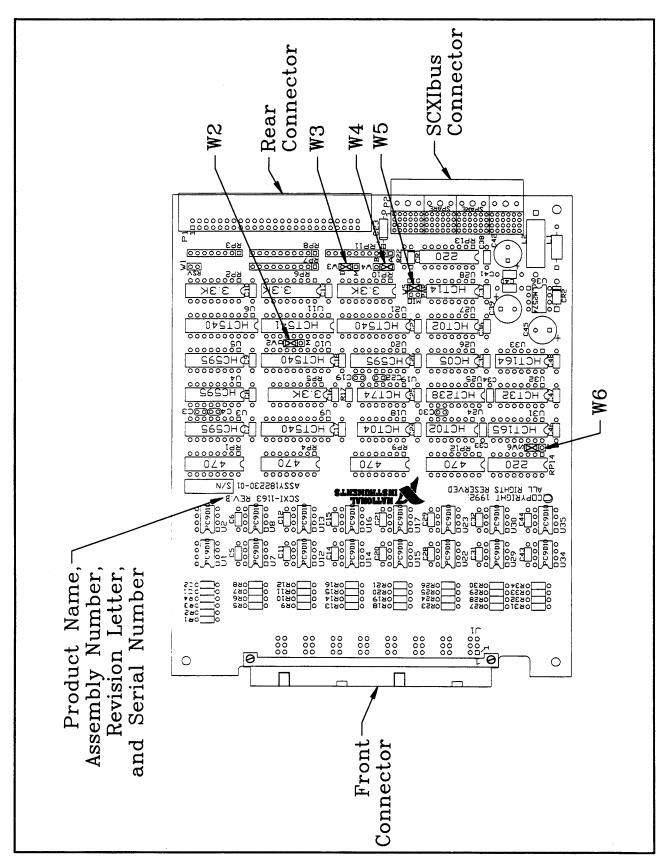


Figure 2-1. SCXI-1163 Parts Locator Diagram

The SCXI-1163 can accept data in two forms—serial and parallel. Serial data is transferred across the SCXIbus using the Serial Peripheral Interface (SPI) protocol. Using serial communication, one data acquisition board that is cabled to one SCXI module in an SCXI system can control the digital communication for all the boards in the system. Parallel data is read from the rear connector and transferred directly to the outputs at the front connector. No extra communication through the rear connector is needed or permitted with parallel communication; thus you can transfer parallel data to the outputs more rapidly than serial data. However, each module that is utilizing parallel data transfers requires a separate data source, such as a data acquisition board.

You can configure the SCXI-1163 to primarily accept either parallel or serial data. In one configuration, the rear connector accepts parallel data; in the other configuration, the rear connector creates a serial communication link with the SCXIbus. Configure the module for parallel data transfers when you want to send data directly from the rear connector to the outputs. Configure the module for serial communication whenever you want to send only serial data to the module. You must configure the module for serial communication if you want a data acquisition board that is cabled to the module rear connector to control the SCXIbus.

When you cable the SCXI-1163 to a data acquisition board, you must also configure the SCXI-1163 to recognize the board either as a DIO-type or an MIO-type board. DIO-type boards are National Instruments boards that have only digital inputs and outputs. These boards include the DIO-24, DIO-32F, and DIO-96. MIO-type boards are National Instruments boards that have both analog and digital inputs and digital outputs. These boards consist of MIO boards; Lab-NB, Lab-PC, Lab-PC+, and Lab-LC boards; and PC-LPM-16 boards. You can use either type for serial communication; for parallel communication, you can use only the DIO-type boards. However, when you use the DIO-24 for *parallel* communication, only channels 0 through 23 can be controlled on the SCXI-1163.

To configure the SCXI-1163 module, use the five user-configurable jumpers shown in the parts locator diagram, Figure 2-1. There is also one reserved jumper that should remain empty. To change the configuration of the module, use the following procedure:

- 1. Remove the grounding screw of the top cover.
- 2. Snap out the top cover of the shield by placing a screwdriver in the groove at the bottom of the module.
- 3. Remove the jumpers to be changed and replace them on the appropriate pins.
- 4. Record the new jumper settings on the *SCXI-1163 Hardware Configuration Form* in Appendix F, *Customer Communication*.
- 5. Snap the top cover back in place.
- 6. Replace the grounding screw to ensure proper shielding.

The following warnings contain important safety information concerning hazardous voltages.

Warnings:

Keep away from live circuits. Do not remove equipment covers or shields unless you are trained to do so. If signal wires are connected to the module or terminal block, dangerous voltages may exist even when the equipment is turned off. To avoid dangerous electrical shock, do not perform procedures involving cover or shield removal unless you are qualified to do so.

Do not operate damaged equipment. The safety protection features built into this module can become impaired if the module becomes damaged in any way. If it is damaged, turn the module off and do not use until service-trained personnel can check its safety. If necessary, return the module to National Instruments for service and repair to ensure that its safety is not compromised.

Do not substitute parts or modify equipment. Because of the danger of introducing additional hazards, do not install unauthorized parts or modify the module. Return the module to National Instruments for service and repair to ensure that its safety features are not compromised.

When using the terminal block with high common-mode voltages, you *must* insulate your signal wires appropriately. National Instruments is *not* liable for any damages or injuries resulting from inadequate signal wire insulation.

When connecting or disconnecting signal lines to the SCXI-1326 terminal block screw terminals, make sure the lines are powered off to prevent shock hazard.

Connections, including power signals to ground and vice versa, that exceed any of the maximum signal ratings on the SCXI-1163 can damage any or all of the boards connected to the SCXI chassis, the host computer, and the SCXI-1163 module. National Instruments *is not liable for any damages or injuries* resulting from incorrect signal connections.

If high voltages (≥42 Vrms) are present, you must connect the safety earth ground to the strain relief tab. This complies with UL 1244 and fully protects against electric shock when the terminal block is not connected to the chassis. To connect the safety earth ground to the strain relief tab, run an earth ground wire in the cable from the signal source to the terminal block. National Instruments is not liable for any damages or injuries resulting from inadequate safety earth ground connections.

Jumper Use

Use the jumpers as follows:

- Reserved jumper
 - Jumper W1 is reserved; do not connect this jumper.
- User-configurable jumpers
 - Jumpers W2 and W3 select whether the SCXI-1163 is to be connected to a DIO-type board or to an MIO-type board. If you are controlling the SCXI-1163 module via the SCXI backplane, the position of these jumpers is irrelevant.
 - Jumper W4 connects a pullup resistor to the SERDATOUT signal on the rear signal connector.

- Jumper W5 carries the SCXIbus MISO line, after buffering, to the SERDATOUT signal on the rear signal connector.
- Jumper W6 selects the primary operating mode, either serial or parallel, and configures the rear connector accordingly.

Further configuration of the board is software controlled and is discussed later in this chapter.

Jumper Configuration

All five user-configurable jumpers (W2 through W6) on the SCXI-1163 are for digital communication between the data acquisition board and the SCXI-1163 module.

The SCXI-1163 has two jumpers, W2 and W3, that indicate to the module what type of data acquisition board is to be connected to the module rear signal connector. The SCXI-1163 also has two jumpers, W4 and W5, for communication between the data acquisition board and the SCXIbus. There is also one jumper, W6, that you use to set the primary mode of operation. See Tables 2-1 and 2-2 for the description and configuration of the jumper settings.

Jumpers W2 and W3

You can use two types of data acquisition boards to communicate with the SCXI-1163–DIO-type boards and MIO-type boards. Jumpers W2 and W3 configure the rear connector to accept signals from either a DIO-type or an MIO-type data acquisition board. Both jumpers have labels indicating the DIO and MIO configurations. If you want to use the SCXI-1163 with a DIO-type board, place the jumpers in the D position. This position is the factory setting. If you want to use the SCXI-1163 with an MIO-type board, place the jumpers in the M position. If you are controlling the SCXI-1163 via the SCXI backplane and are not using the rear connector, the position of these jumpers is irrelevant.

Jumper W4

Position A connects a 2.2 k Ω pullup resistor to the SERDATOUT line. This is the factory-default setting. Position B does not connect the pullup resistor to the SERDATOUT line.

Jumper W5

Position DIO connects the SCXIbus MISO line, after buffering, to the SERDATOUT pin of the rear signal connector when used with a DIO-type board. Position MIO connects the SCXIbus MISO line, after buffering, to the SERDATOUT pin of the rear signal connector when used with an MIO-type board. In these settings, when you have set jumper W4 properly, the data acquisition board can read the Module ID Register or the Status Registers of the SCXI-1163. See the *Timing Requirements and Communication Protocol* section later in this chapter, and Chapter 4, *Register Descriptions*, for information on reading the Module ID Register and the Status registers. See Appendix E, *SCXI-1163 Cabling*, for the pin equivalences of the SCXI-1163 rear signal connector and the data acquisition board I/O connector. The factory-default setting is position DIO.

Position PAR disconnects SERDATOUT from the SCXIbus MISO line. Use this position when you will connect the module in parallel to a data acquisition board.

Using Jumpers W4 and W5

If a module is not connected to a data acquisition board, the positions of jumpers W4 and W5 are irrelevant. Jumpers W4 and W5 give the data acquisition board access to the MISO line on the backplane. You use the MISO line to read the Module ID Register of modules. National Instruments software does not use this ability. You must indicate to the software which module is in which slot. In addition to reading the Module ID Register, you can use the MISO line on the SCXI-1163 to read the Status Registers, which indicate the primary and output modes of operation. National Instruments software uses this feature.

The SERDATOUT line is driven with an open-collector driver, which is a driver that actively drives low or goes to a high-impedance state, relying on a pullup resistor to make the signal line go high. When using a single chassis, set jumper W4 to position A on the SCXI-1163 that is connected to the data acquisition board and set jumper W5 to DIO or MIO. In this setting, the module drives MISO to SERDATOUT and connects the necessary pullup resistor to the SERDATOUT line. When using multiple chassis, set jumper W5 to position DIO or MIO on all of the SCXI-1163s that are cabled to the data acquisition board. Only one of the SCXI-1163s that are cabled to the data acquisition board should have jumper W4 in position A. It does not matter which of the SCXI-1163s that are cabled to the data acquisition board has the pullup connected. You should set jumper W4 to position B on all of the other SCXI-1163 modules that are cabled to the data acquisition board. If you attach too many pullup resistors to the SERDATOUT line, the drivers cannot drive the line low.

Jumper W6

Jumper W6 sets the primary mode of operation to either serial mode or parallel mode and configures the rear connector accordingly. With the primary mode of operation set to parallel, the rear connector is configured to accept parallel data from a DIO board. With the primary mode of operation set to serial, the rear connector is configured to allow serial communication between a data acquisition board and the SCXIbus.

To set the primary mode of operation to parallel, set jumper W6 to position P. In this mode, jumper W5 should be set to PAR to prevent the MISO line from inadvertently driving one of the outputs. To set the primary mode of operation to serial, set jumper W6 to position S.

Table 2-1. Configuration of Jumpers W2, W3, and W5 for DIO-Type and MIO-Type Boards

| Jumper | Description | Configuration for DIO-Type Board | Configuration for MIO-Type Board |
|----------|---|----------------------------------|----------------------------------|
| W2 | Configures rear connector— Factory setting is for DIO-type boards | D M | D · M |
| W3 | Configures rear connector— Factory setting is for DIO-type boards | D M | D · M |
| W5 W5 | Connects MISO to SERDATOUT on a DIO-type or MIO-type board–Factory setting is for DIO-type boards | DIO DIC PAR OIV | OIW PAR OIF |
| | Parking position–Disconnects MISO from SERDATOUT | ≥ PAR | ≥ PAR |

Table 2-2. Configuration of Jumpers W4 and W6

| Jumper | Description | Configuration |
|--------|--|------------------|
| W4 | Factory Setting–Connects pullup to SERDATOUT | B A |
| W4 | Parking position | B · A |
| W6 | Sets primary mode of operation to parallel | S |
| W6 | Factory setting—Sets primary mode of operation to serial | P S L P |

Hardware Installation

You can install the SCXI-1163 in any available SCXI chassis. After you have made any necessary changes and have verified and recorded the jumper settings on the form in Appendix F, *Customer Communication*, you are ready to install the SCXI-1163. The following are general installation instructions, but consult the user manual or technical reference manual of your SCXI chassis for specific instructions and warnings.

- 1. Turn off the computer that contains the data acquisition board or disconnect the computer from your SCXI chassis.
- 2. Turn off the SCXI chassis. Do not insert the SCXI-1163 into a chassis that is turned on.
- 3. Insert the SCXI-1163 into the board guides. Gently guide the module into the back of the slot until the connectors make good contact. If you have already installed a cable assembly in the rear of the chassis, you must firmly engage the module and cable assembly; however, do not *force* the module into place.
- 4. Screw the front mounting panel of the SCXI-1163 to the top and bottom threaded strips of your SCXI chassis.
- 5. If this module is to be connected to an MIO-16 or to a DIO-24 data acquisition board, attach the connector at the metal end of the SCXI-1340 cable assembly to the rear signal connector on the SCXI-1163 module. Screw the rear panel to the rear threaded strip. Attach the loose end of the cable to the MIO-16 or DIO-24 board.

Note: For installation procedures with other SCXI accessories and data acquisition boards, consult Appendix E, *SCXI-1163 Cabling*.

- 6. Check the installation.
- 7. Turn on the SCXI chassis.
- 8. Turn on the computer or reconnect the computer to your chassis.

The SCXI-1163 board is installed and ready for operation.

Signal Connections

This section describes the signal connections to the SCXI-1163 board via the SCXI-1163 front connector and rear signal connector, and includes specifications and connection instructions for the signals given on the SCXI-1163 connectors.

Warning:

Connections that exceed any of the maximum ratings of input signals on the SCXI-1163 can damage the SCXI-1163 board and the SCXIbus. Maximum input ratings for each signal are given in this chapter under the discussion of that signal. National Instruments is *not* liable for any damages resulting from signal connections that exceed these ratings.

Front Connector

Figure 2-2 shows the pin assignments for the SCXI-1163 front connector.

| Pin Number | Signal Name | Co A | olum B | n C | Signal Name |
|---------------|----------------------------------|---------------|-----------|--------|----------------|
| 30 | Out 0 · Out 1 · Out 2 · | | | | ·Vcc |
| 29 | Out 3 · | | ه ا | • | GND |
| 26 25 | Out 5 · Out 6 · Out 7 · | -° | ٦ ا | • | · Vcc · GND |
| 22 | Out 8 · Out 9 · Out 10 · | -0 | ļ | • | Vcc |
| 21 | Out 11 | +° | ļ | • | GND |
| 18 | Out 12 · Out 13 · Out 14 · | • | 了 一 | • | Vcc |
| 17 | Out 15 | | } | • | GND |
| 14 | Out 19 · Out 18 · Out 17 · | | _ | • | GND |
| 13 | Out 16 | ightharpoonup | _ _ | • | Vcc |
| 10 | Out 23 · Out 22 · Out 21 · | - | \ | • | GND |
| 9 | Out 20 | ightharpoonup | _ _ | • | Vcc |
| 6 | Out 27 · Out 26 · Out 25 · | ightharpoonup | 了 一 | • | GND |
| 5 | Out 24 | | } | • | Vcc |
| 2 | Out 31 · Out 30 · Out 29 · | • | つ | • | GND |
| 1 | Out 28 | <u></u> | | • | Vcc |

Figure 2-2. SCXI-1163 Front Connector Pin Assignment

Front Connector Signal Descriptions

| Pin | Signal Name | Description |
|-----------------------|-------------|----------------|
| B30, A30, B29, A29 | Out<03> | Port 0 outputs |
| C30 | Vcc | Port 0 power |
| C29 | GND | Port 0 ground |
| B26, A26, B25, A25 | Out<47> | Port 1 outputs |
| C26 | Vcc | Port 1 power |
| C25 | GND | Port 1 ground |
| B22, A22, B21, A21 | Out<811> | Port 2 outputs |
| C22 | Vcc | Port 2 power |
| C21 | GND | Port 2 ground |
| B18, A18, B17, A17 | Out<1215> | Port 3 outputs |
| C18 | Vcc | Port 3 power |
| C17 | GND | Port 3 ground |
| A13, B13, A14, B14 | Out<1619> | Port 4 outputs |
| C14 | GND | Port 4 ground |
| C13 | Vcc | Port 4 power |
| A9, B9, A10, B10 | Out<2023> | Port 5 outputs |
| C10 | GND | Port 5 ground |
| C9 | Vcc | Port 5 power |
| A5, B5, A6, B6 | Out<2427> | Port 6 outputs |
| C6 | GND | Port 6 ground |
| C5 | Vcc | Port 6 power |

| Pin | Signal Name | Description (continued) |
|-------------------|-------------|--------------------------------|
| A1, B1, A2, B2 | Out<2831> | Port 7 outputs |
| C2 | GND | Port 7 ground |
| C1 | Vcc | Port 7 power |

The SCXI-1163 consists of eight ports of four optically isolated digital outputs. Each port of outputs has a separate connection for a +5 V power supply (Vcc) and for a ground (GND) for that port. Digital logic powered by the port Vccs and referenced to the port grounds drives the outputs of each port; therefore, for any port of outputs to work, you must connect a Vcc and a ground to that particular port. The outputs work on a +5 V supply (in other words, Vcc must be 5 V above ground for any given port), and supply voltages of 7 V or more may damage the output circuitry. It is recommended you keep the Vcc between 4.5 and 5.5 V above ground. The Vcc, ground, and four outputs of one port are isolated from the Vcc, ground, and four outputs of any other port, as well as from the internal circuitry of the module.

All signals have a working isolation voltage of 450 VAC or VDC referenced to chassis earth ground and to signals of other ports. *There is no isolation barrier between signals of the same port.* The signal-to-ground and port-to-port breakdown voltage is 1,900 Vrms.

Terminal Block

To connect the signals to the SCXI-1163 outputs, you can use a National Instruments terminal block with screw terminals for easy connection.

The terminal block kit is listed in the *Optional Equipment* section in Chapter 1, *Introduction*.

SCXI-1326 Terminal Block

The SCXI-1326 front terminal block consists of a shielded board with supports to connect it to the SCXI-1163 front connector. Forty-eight screw terminals are available for easy signal connection.

When connecting your signals to the SCXI-1326 for use with the SCXI-1163, you should follow the labeling as indicated in Figure 2-3, SCXI-1326 Parts Locator Diagram.

The following warnings contain important safety information concerning hazardous voltages.

Warnings:

If high voltages (≥42 Vrms) are present, you must connect the safety earth ground to the strain relief tab. This complies with UL 1244 and fully protects against electric shock when the terminal block is not connected to the chassis. To connect the safety earth ground to the strain relief tab, run an earth ground wire in the cable from the signal source to the terminal block. National Instruments is not liable for any damages or injuries resulting from inadequate safety earth ground connections.

When using the terminal block with high common-mode voltages, you *must* insulate your signal wires appropriately. National Instruments is *not* liable for any damages or injuries resulting from inadequate signal wire insulation.

When connecting or disconnecting signal lines to the SCXI-1326 terminal block screw terminals, make sure the lines are powered off to prevent shock hazard.

Connections, including power signals to ground and vice versa, that exceed any of the maximum signal ratings on the SCXI-1163 can damage any or all of the boards connected to the SCXI chassis, the host computer, and the SCXI-1163 module. National Instruments is not liable for any damages or injuries resulting from incorrect signal connections.

Signal Connection

To connect the signal to the terminal block, use the following procedure:

- 1. Remove the grounding screw of the top cover.
- 2. Snap out the top cover of the shield by placing a screwdriver in the groove at the bottom of the terminal block.
- 3. Slide the signal wires one at a time through the front panel strain relief. You can add insulation or padding if necessary.
- 4. Connect the wires to the screw terminals, making sure you connect a Vcc and a ground to every port you use.
- 5. Tighten the strain relief by tightening the larger screws.
- 6. Snap the top cover back in place.
- 7. Replace the grounding screw to ensure proper shielding.
- 9. Connect the terminal block to the SCXI-1163 front connector as explained in the *SCXI-1326 Installation* section, the next section in this chapter.

Figure 2-3 shows a parts locator diagram for the SCXI-1326 terminal block.

Warning:

If high voltages (≥42 Vrms) are present, you must connect the safety earth ground to the strain relief tab. This complies with UL 1244 and fully protects against electric shock when the terminal block is not connected to the chassis. To connect the safety earth ground to the strain relief tab, run an earth ground wire in the cable from the signal source to the terminal block. National Instruments is not liable for any damages or injuries resulting from inadequate safety earth ground connections.

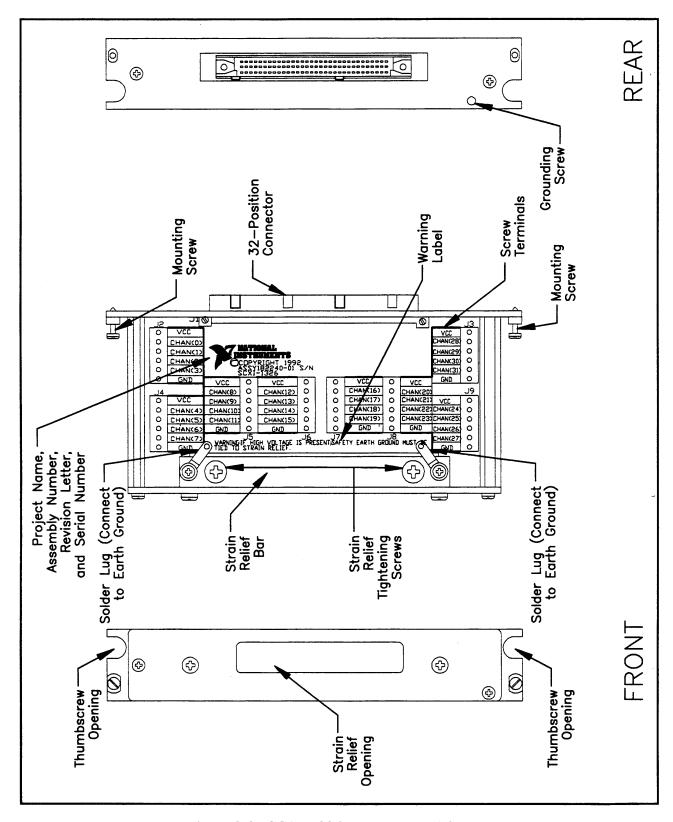


Figure 2-3. SCXI-1326 Parts Locator Diagram

SCXI-1326 Installation

To connect the terminal block to the SCXI-1163 front connector, follow these steps:

- 1. Connect the SCXI-1163 front connector to its mating connector on the terminal block.
- 2. Make sure that the SCXI-1163 top and bottom thumbscrews do not obstruct the rear panel of the terminal block.
- 3. Tighten the top and bottom screws on the back of the terminal block to hold the terminal block securely in place.

Rear Signal Connector

Note: If you will be using the SCXI-1163 with a National Instruments data acquisition board and cable assembly, you do not need to read the remainder of this chapter. If you will also be using the SCXI-1180 feedthrough panel or the SCXI-1343 rear screw terminal adapter with the SCXI-1163, you should read this section.

The rear signal connector is configured based on the jumper settings described earlier in this chapter. Jumper W6 determines whether the rear connector will be used for serial or parallel communication. If you set jumper W6 to serial, jumpers W2, W3, and W5 determine whether the rear connector is configured for an MIO-type connection or a DIO-type connection.

Figure 2-4A shows the pin assignments for the SCXI-1163 rear signal connector configured for serial communication. Figure 2-4B shows the pin assignments for the rear signal connector configured for parallel communication.

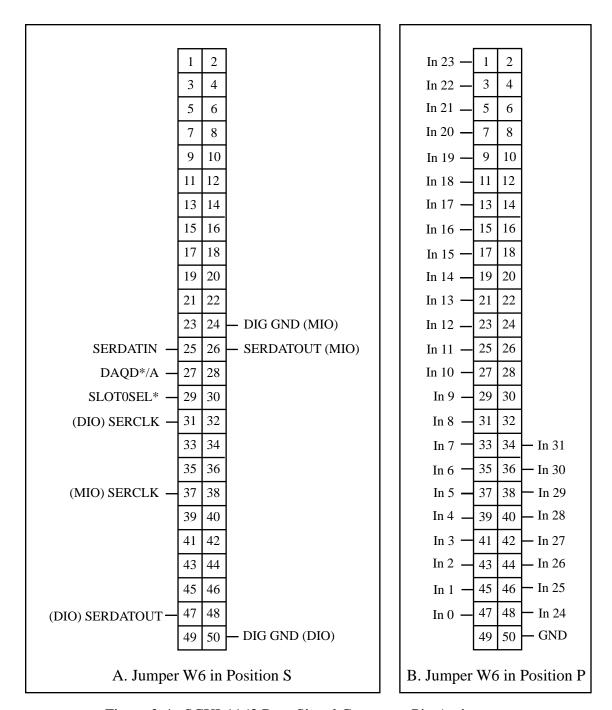


Figure 2-4. SCXI-1163 Rear Signal Connector Pin Assignment

Rear Signal Connector Signal Descriptions, Serial Configuration

| Pin | Signal Name | Description |
|----------|-------------|---|
| 24 or 50 | DIG GND | Digital Ground – Supplies the reference for data acquisition board digital signals and is tied to the module digital ground. Pin 50 is for DIO-type boards. Pin 24 is for MIO-type boards. Jumper W3 selects the pin. |
| 25 | SERDATIN | Serial Data In – Taps into the SCXIbus MOSI line to provide serial input data to a module or Slot 0. |
| 26 or 47 | SERDATOUT | Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module. Pin 47 is for DIO-type boards. Pin 26 is for MIO-type boards. Jumper W5 selects the pin. |
| 27 | DAQD*/A | Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information. |
| 29 | SLOT0SEL* | Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is sent to a module or to Slot 0. |
| 31 or 37 | SERCLK | Serial Clock – Taps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines. Pin 31 is for DIO-type boards. Pin 37 is for MIO-type boards. Jumper W2 selects the pin. |

^{*} Indicates active low.

All other pins are not connected.

See the *Timing Requirements and Communication Protocol* section later in this chapter for more detailed information on timing.

Rear Signal Connector Signal Descriptions, Parallel Configuration

| Pin | Signal Name | Description |
|--|-------------|--|
| 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23, 21, 19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 48, 46, 44, 42, 40, 38, 36, 34 | In <031> | Digital Inputs – The logic levels at these inputs determine the output states. |
| 50 | GND | Ground – Supplies ground reference for the parallel inputs. |

All other pins are not connected.

The signals on the rear signal connector are digital I/O signals. Signal connection guidelines for each of these groups are given in the following section.

Serial I/O Signal Connections

Pins 24 through 27, 29, 31, 37, 47, and 50 constitute the digital I/O lines of the rear signal connector when it is configured for serial communication. The lines are divided into three categories—the digital input signals, the digital output signals, and the digital timing signals.

The digital input signals are pins 24 or 50, 25, 27, 29, and 31 or 37. The data acquisition board uses these pins to configure the SCXI module that is under data acquisition board control. Each digital line emulates the SCXIbus communication signals as follows:

- Pin 24 or 50 is the digital ground reference for the data acquisition board digital signals and is tied to the module digital ground. Pins 24 and 50 are *not* tied together.
 - Pin 24 is for MIO-type boards when SCXI-1163 jumpers W2 and W3 are in the MIO position.
 - Pin 50 is for DIO-type boards when SCXI-1163 jumpers W2 and W3 are in the DIO position.
- Pin 25 is SERDATIN and is equivalent to the SCXIbus MOSI serial data input line.
- Pin 27 is DAQD*/A and is equivalent to the SCXIbus D*/A line. It indicates to the module whether the incoming serial stream on SERDATIN is data (DAQD*/A = 0) or address (DAQD*/A = 1) information.
- Pin 29 is SLOT0SEL* and is equivalent to the SCXIbus INTR* line. It indicates whether the data on the SERDATIN line is being sent to Slot 0 (SLOT0SEL* = 0) or to a module (SLOT0SEL* = 1).
- Pin 31 or 37 is SERCLK and is equivalent to the SCXIbus SPICLK line. Either pin clocks the serial data on the SERDATIN line into the module registers. Pins 31 and 37 are *not* tied together.
 - Pin 31 is for DIO-type boards when SCXI-1163 jumpers W2 and W3 are in the DIO position.
 - Pin 37 is for MIO-type boards when SCXI-1163 jumpers W2 and W3 are in the MIO position.

The digital output signal is pin 26 or 47:

- Pin 26 or 47 is SERDATOUT and is equivalent to SCXIbus MISO when jumper W5 is in either the MIO or DIO position. Pins 26 and 47 are *not* tied together.
 - Pin 26 is for MIO-type boards when SCXI-1163 jumpers W2 and W3 are in the MIO position.
 - Pin 47 is for DIO-type boards when SCXI-1163 jumpers W2 and W3 are in the DIO position.

When you configure the SCXI-1163 for an MIO-type board, the digital I/O signals of the SCXI-1163 match the digital I/O lines of the MIO board. When you use the SCXI-1163 with an SCXI-1341, SCXI-1342, or SCXI-1344 cable assembly, the SCXI-1163 signals match the digital lines of the Lab-NB/Lab-PC/Lab-PC+ boards, the PC-LPM-16 board, and the Lab-LC board, respectively. When you configure the SCXI-1163 for a DIO-type board, the digital I/O signals of the SCXI-1163 match the digital I/O lines of the DIO-24 and DIO-96. When used with an SCXI-1348 cable assembly, the SCXI-1163 signals match the digital lines of the DIO-32F.

Table 2-3 lists the pin equivalences. For more information, consult Appendix E, *SCXI-1163 Cabling*.

Table 2-3. SCXIbus to SCXI-1163 Rear Signal Connector to Data Acquisition Board Pin Equivalences

| SCXIbus Line | SCXI-1163 Rear Signal Connector | MIO Boards | Lab-NB/Lab-PC/ Lab-PC+/Lab-LC | PC-LPM-16 | DIO-24 | 96-OIQ | DIO-32F |
|--------------|------------------------------------|------------|----------------------------------|-----------|--------|--------|---------|
| MOSI | SERDATIN | ADIO0 | PB4 | DOUT4 | PB3 | APB3 | DIOB3 |
| D*/A | DAQD*/A | ADIO1 | PB5 | DOUT5 | PB2 | APB2 | DIOB2 |
| INTR* | SLOT0SEL* | ADIO2 | PB6 | DOUT6 | PB1 | APB1 | DIOB1 |
| SPICLK | SERCLK | EXTSTROBE* | PB7 | DOUT7 | PB0 | APB0 | DIOB0 |
| MISO | SERDATOUT | BDIO0 | PC1 | DIN6 | PA0 | APA0 | DIOA0 |

The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage

input rating 5.5 V with respect to DIG GND

Digital input specifications (referenced to DIG GND):

V_{IH} input logic high voltage 2 V minimum V_{II} input logic low voltage 0.8 V maximum

 $I_{\rm I}$ input current leakage $\pm 1 \,\mu A$ maximum

Digital output specifications (referenced to DIG GND):

V_{OH} output logic high voltage 3.7 V minimum at 4 mA maximum V_{OL} output logic low voltage 0.4 V maximum at 4 mA maximum

Timing Requirements and Communication Protocol

Communication Signals

This section describes the methods for communicating on the Serial Peripheral Interface (SPI) bus and their timing requirements. The communication signals are SERDATIN, DAQD*/A, SLOTOSEL*, SERDATOUT, and SERCLK. Because SS* is produced by Slot 0 according to data acquisition board programming, this section also discusses SS* timing relationships. For information on the Slot 0 Slot-Select Register, consult Chapter 4, *Register Descriptions*.

The data acquisition board writes a slot-select number to Slot 0 to determine to which slot it will talk. In the case of an SCXI-1001 chassis, this write also determines to which chassis the data acquisition board will talk.

Use the following procedure for selecting a slot in a particular chassis. Figure 2-5 shows the timing of this procedure with the example of selecting Slot 11 in Chassis 9. Notice that the factory-default chassis address for the SCXI-1000 is address 0. For information on changing the address of your chassis, consult the *SCXI-1000/1001 User Manual*. An SCXI-1000 chassis will respond to any chassis number.

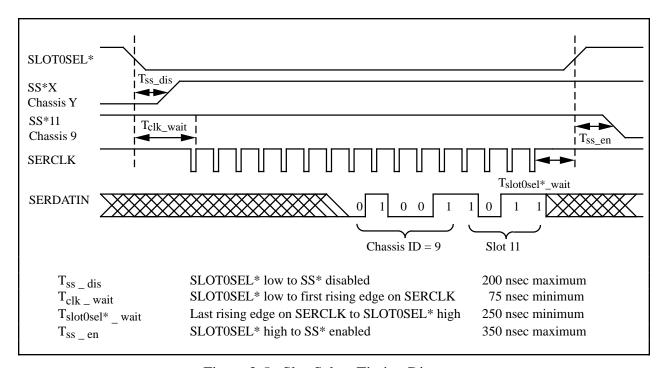


Figure 2-5. Slot-Select Timing Diagram

To write the 16-bit slot-select number to Slot 0, follow these steps:

1. Initial conditions:

```
SERDATIN = don't care.
DAQD*/A = 1.
SLOT0SEL* = 1.
SERCLK = 1.
```

- 2. Clear SLOTOSEL* to 0. This deasserts all SS* lines to all modules in all chassis.
- 3. For each bit, starting with the MSB, perform the following action:
 - a. SERDATIN = bit to be sent. These bits are the data that are being written to the Slot-Select Register.
 - b. SERCLK = 0.
 - c. SERCLK = 1. This rising edge clocks the data.
- 4. Set to 1. This asserts the SS* line of the module whose slot number was written to Slot 0. If you are using multiple chassis, only the appropriate slot in the chassis whose address corresponds to the written chassis number is selected. When no communication is taking place between the data acquisition board and any modules, write zero to the Slot-Select Register to ensure that no accidental writes occur.

Figure 2-6 shows the timing requirements on the SERCLK and SERDATIN signals. You must observe these timing requirements for all communications. T_{delay} is a specification of the SCXI-1163.

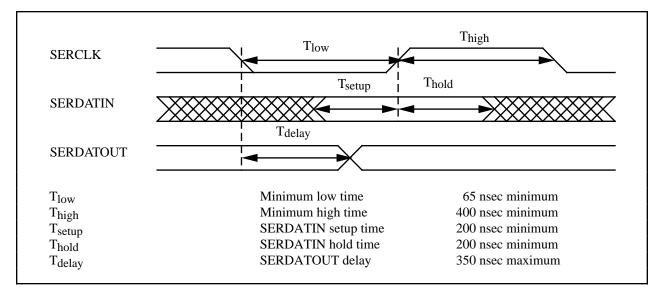


Figure 2-6. Serial Data Timing Diagram

After you select the module slot as previously described, each write or read cycle to the module requires you to write first to the Address Handler, then to the register of interest.

To write to the Address Handler, follow these steps:

1. Initial conditions:

SS* asserted low.
SERDATIN = don't care.
DAQD*/A = 1 (indicates data will be written to the Address Handler).
SLOT0SEL* = 1.
SERCLK = 1 (and has not transitioned since SS* went low).

2. For each bit to be written, and starting with the MSB, perform the following actions (these bits are the address of the register of interest):

Establish the desired SERDATIN level corresponding to this bit. SERCLK = 0. SERCLK = 1. This rising edge clocks the data.

3. Pull DAQD*/A low to deselect the Address Handler and select the register that had its address written to the Address Handler. This selects a register for writing to or reading from.

Figure 2-7 illustrates a write to the SCXI-1163 Address Handler of the binary pattern:

00000000 00000001

This pattern is the address of the Data Register.

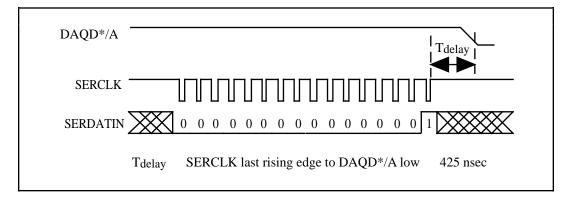


Figure 2-7. Address Handler Timing Diagram

After the Address Handler has been written to, an address line of a register has been asserted. At that stage you can write to the SCXI-1163 Data Register and read from its Module ID Register or Status Registers using the following protocols. The contents of the Module ID Register are reinitialized by deasserting Slot-Select. After the 32 bits of data are read from the Module ID Register, further data will be zeros until reinitialization occurs. The Data Register latches its data to the outputs when it is deselected.

To write to the Data Register, follow these steps:

1. Initial conditions:

SS* asserted low.
SERDATIN = don't care.
DAQD*/A = 0 (indicates data will be written to a Register).
SLOT0SEL* = 1.
SERCLK = 1 (and has not transitioned since DAQD*/A went low).

2. For each bit to be written:

Establish the desired SERDATIN level corresponding to this bit. SERCLK = 0.

SERCLK = 1. This rising edge clocks the data.

- 3. Pull DAQD*/A high. This disables further writes to the module Data Register and latches the information to the outputs. If you want, you can write address FFFF (hexadecimal) to the Address Handler. This selects the Parking Register and makes the module registers more immune to noise.
- 4. Pull low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 5. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register.

Figure 2-8 illustrates a write to the SCXI-1163 Data Register of the binary pattern:

10000011 00001111 00000000 00000000

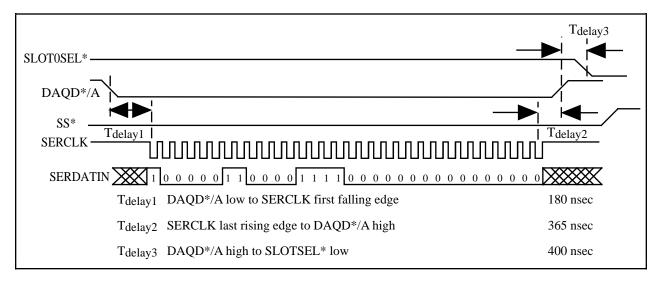


Figure 2-8. Data Register Write Timing Diagram

To read from the Module ID Register, follow these steps:

1. Initial conditions:

```
SS* asserted low.
SERDATIN = don't care.
DAQD*/A = 0.
= 1.
SERCLK = 1 (and has not changed since DAQD*/A went low).
```

2. For each bit to be read:

```
SERCLK = 0.
SERCLK = 1. This rising edge clocks the data.
Read the level of the SERDATOUT line.
```

- 3. Pull DAQD*/A high. This disables further reads from the Module ID Register. If you want, you can write address FFFF (hexadecimal) to the Address Handler. This selects the Parking Register and makes the module registers more immune to noise.
- 4. Pull low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 5. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register.

Figure 2-9 illustrates a read of the SCXI-1163 Module ID Register.

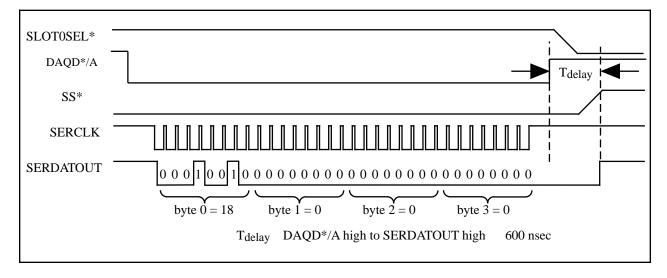


Figure 2-9. SCXI-1163 Module ID Register Timing Diagram

To read from a Status Register, follow these steps:

1. Initial conditions:

```
SS* asserted low.

SERDATIN = don't care.

DAQD*/A = 0.

= 1.

SERCLK = don't care.
```

2. The Status Registers are 1-bit read-only registers that indicate the primary or jumper-set mode of operation and the mode of operation currently driving the outputs. The register at address 0002 holds the Primary Mode Status; the register at address 0003 holds the Output Mode Status. You do not need to pulse the SERCLK to read the Status Register.

Read the level of the SERDATOUT line. The level can be interpreted as follows:

- Primary Mode Status Register—a 1 indicates that the primary mode of operation is set for parallel writes, and a 0 indicates that the primary mode of operation is set for serial writes.
- Output Mode Status Register—a 1 indicates that the outputs are being set by the data contents of the data register, and a 0 indicates that the outputs are being set by the levels seen at the rear connector.
- 3. Pull DAQD*/A high. This disables further reads from the Status Register. If you want, you can write address FFFF (hexadecimal) to the Address Handler. This selects the Parking Register and makes the module registers more immune to noise.
- 4. Pull low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 5. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register.

Figure 2-10 illustrates a read of an SCXI-1163 Status Register.

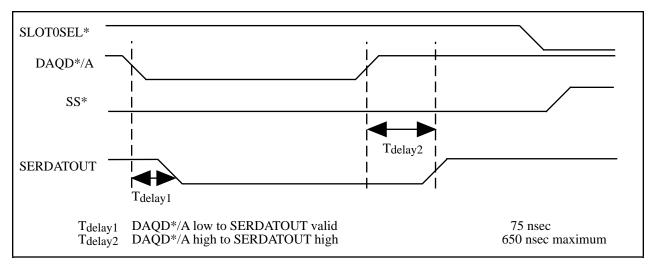


Figure 2-10. SCXI-1163 Status Register Timing Diagram

For further details on programming these signals, refer to Chapter 5, *Programming*.

Chapter 3 Theory of Operation

This chapter contains a functional overview of the SCXI-1163 module and explains the operation of each functional unit making up the SCXI-1163.

Functional Overview

The block diagram in Figure 3-1 shows the key functional components of the SCXI-1163.

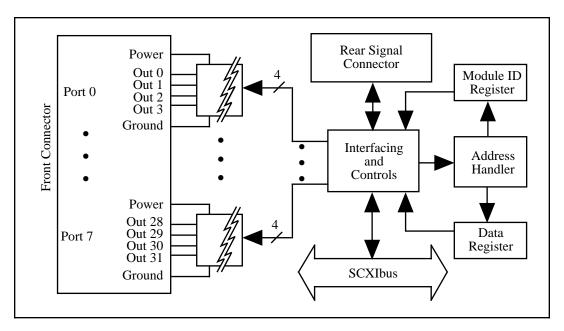


Figure 3-1. SCXI-1163 Block Diagram

The major components of the SCXI-1163 are as follows:

- The SCXIbus connector
- The interface and routing circuitry
- The register circuitry
- The optically isolated output channels

SCXIbus Connector

Figure 3-2 shows the pinout of the SCXIbus connector.

Theory of Operation Chapter 3

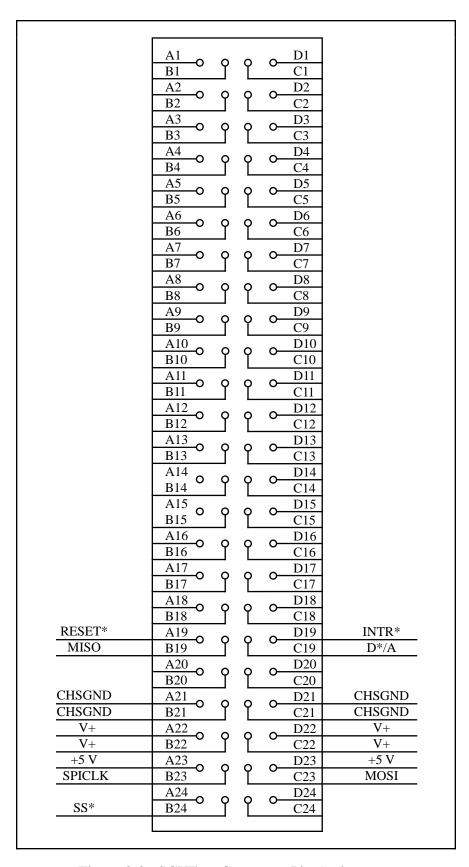


Figure 3-2. SCXIbus Connector Pin Assignment

Chapter 3 Theory of Operation

SCXIbus Connector Signal Descriptions

| Pin | Signal Name | Description |
|-----------------------|-------------|--|
| A19 | RESET* | Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input. |
| B19 | MISO | Master-In-Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O. |
| C19 | D*/A | Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O. |
| D19 | INTR* | Interrupt – Active low. Causes data that is on MOSI to be written to the Slot 0 Slot-Select Register. Open collector. Output. |
| A21, B21, C21, D21 | CHSGND | Chassis Ground – Digital and analog ground reference. |
| A22, B22, C22, D22 | V+ | Positive Supply – +18.5 to +25 V. |
| A23, D23 | +5 V | +5 VDC Source – Digital power supply. |
| B23 | SPICLK | Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O. |
| C23 | MOSI | Master-Out-Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O. |
| B24 | SS* | Slot Select – When low, enables module communication over the SCXIbus. Totem pole. Input. |

^{*} Indicates active low.

All other pins are not connected.

MOSI, MISO, SPICLK, and SS* form a synchronous communication link that conforms with SPI using an idle-high clock and second-edge data latching. D^*/A , INTR*, and RESET* are additional control signals.

When the module is in an SCXI-1000 or SCXI-1001 chassis, the data acquisition board must tap into the open-collector backplane signal lines via the module rear signal connector as a master to write to the module. You must set the jumpers to serial mode and configure them for a DIO board or an MIO board as needed to create this interface. Table 3-1 shows the signal connections from the rear signal connector to the backplane.

Theory of Operation Chapter 3

| Rear Signal Connector Signal | SCXIbus Equivalent |
|---------------------------------|--------------------|
| SERDATIN | MOSI |
| DAQD*/A | D*/A |
| SLOT0SEL* | INTR* |
| SERCLK | SPICLK |
| SERDATOUT | MISO |

Table 3-1. SCXIbus Equivalents for Rear Signal Connector

When the primary mode of operation is jumper configured to serial mode, the SCXI-1163 module converts the data acquisition board signals to open-collector signals on the backplane of the SCXI chassis. For the data acquisition board to talk to a slot, the board must first assert the SS* for that slot. To do this, assert INTR* low, write a 16-bit number over MOSI corresponding to the desired slot (and chassis if you are using an SCXI-1001 chassis), and release INTR* high. At this point, the SS* of the desired slot is asserted low and the data acquisition board can communicate with the module in that slot according to the SPI protocol.

Interface and Routing Circuitry

Figure 3-3 shows a diagram of the SCXI-1163 and SCXIbus digital interface circuitry.

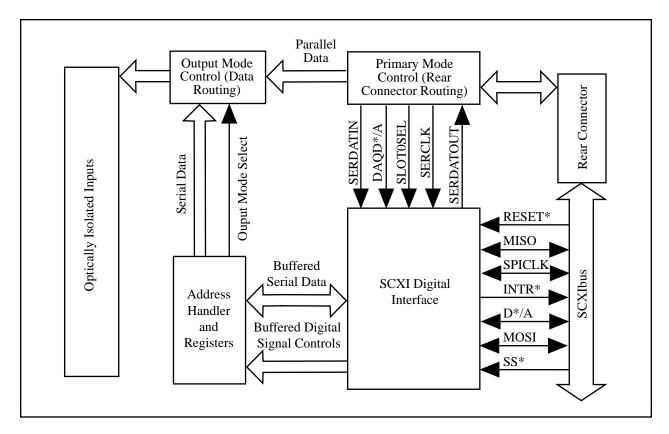


Figure 3-3. Digital Interface and Routing Circuitry Block Diagram

Chapter 3 Theory of Operation

This circuitry is divided into an SCXI digital interface section and two signal routing sections. The SCXI digital interface buffers signals from the SCXIbus to the module and drives signals from the module onto the SCXIbus.

The rear connector routing circuit determines the function of the rear connector from the jumper-configured primary operating mode. When the primary operating mode is serial, the signals from the rear connector are routed to the SCXI digital interface. When the primary operating mode is parallel, the signals from the rear connector are routed to the data router.

The data routing circuit determines the output mode of operation from the Address Handler and registers. When the output mode is set to serial, the outputs get their signals routed from the Data Register. When the output mode is set to parallel, the outputs get their signal routed from the rear connector circuit. Notice that, because the rear connector signals are not routed to the data routing circuit when the primary mode of operation is serial, the output mode of operation cannot be parallel when the primary mode is set to parallel. For additional descriptions of primary and output modes of operation, see Chapter 4, *Register Descriptions*.

Register Circuitry

Figure 3-4 diagrams the SCXI-1163 register circuitry.

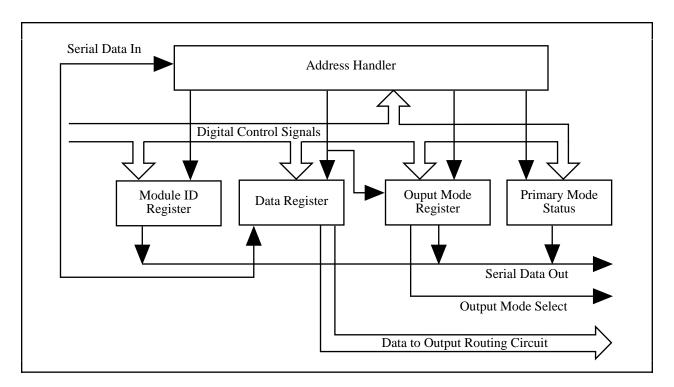


Figure 3-4. SCXI-1163 Register Circuitry

Theory of Operation Chapter 3

The register circuitry section consists of the Data Register, the Module ID Register, the Output Mode Register, and the Primary Mode Status Register.

The Data Register is a 4-byte serial-in parallel-out shift register. Data is received on the MOSI line from either Slot 0 or the data acquisition board when SS* is enabled, D*/A indicates data transfer (D*/A low), and the Data Register address was selected in the Address Handler. When the output mode of operation is set to serial, the Data Register controls the state of the SCXI-1163 outputs. Two addresses can access the Data Register–0001 and 0006 (hexadecimal). Selecting 0001 will set the output mode to serial, and selecting 0006 will return the output mode to the primary mode. The complete descriptions of the register bits are given in Chapter 4, *Register Descriptions*. Writes to the Data Register require the following steps:

- 1. SS* goes low, enabling communication with the board.
- 2. Write 0001 or 0006 (hexadecimal) to the Address Handler. This selects the Data Register.
- 3. D*/A goes low, indicating that the information sent on the MOSI line is data.
- 4. The serial data is available on MOSI and SPICLK clocks it into the register.
- 5. SS* goes high and D*/A goes high, indicating an end of communication. This action latches the Data Register bits.

At reset or at power up, the states of the outputs of the Data Register are set to logic states.

The Module ID Register connects to MISO on the SCXIbus. The Module ID Register is a read-only 4-byte parallel-in serial-out shift register and an SPI communication adapter. The address of the Module ID Register is hex 0000. The contents of the Module ID Register are written onto MISO during the first four bytes of transfer after selecting the Module ID Register in the Address Handler. Zeros are written to MISO thereafter until the Module ID Register is deselected. The SCXI-1163 module ID is hex 00000012.

The Output Mode Register is a 1-bit register that determines the output mode of operation. Set it to serial mode by writing to the Data Register at address 0001; write to address 0006 to return to the primary mode of operation. You can read the output mode by selecting address 0003, pulling D*/A low, and reading the value on the MISO line. A logic low indicates that the output mode is set to parallel, whereas a logic high indicates that the output mode is set to serial.

The Primary Mode Status Register is a read-only register which returns the jumper-configured primary mode of operation. To read the primary mode, select address 0002, pull D*/A low, and read the value on the MISO line. A logic low indicates that the primary mode is set to serial, whereas a logic high indicates that the primary mode is set to parallel.

Optically Isolated Output Channels

The SCXI-1163 consists of eight ports of four optically isolated digital outputs. Each port of outputs has an isolated connection for the Vcc and ground. The outputs of each port are referenced to their particular grounds and powered by their particular Vccs; therefore, for any port of outputs to work, a Vcc and a ground must be connected to that particular port. The Vcc, ground, and four outputs of one port are isolated from the Vcc, ground, and four outputs of any other port, and are isolated from the internal circuitry of the module. Vcc should be 5 V ±.5 V above the ground for a given port. Figure 3-5 represents one of the optically isolated

Chapter 3 Theory of Operation

output channels and the Vcc and ground connections. Table 3-2 shows the channel and port assignments.

These outputs are open-collector outputs with 4.7 k Ω pullups, which can sink 12 mA while maintaining an output voltage below 0.6 V. The rise time of the outputs is 1 µsec into a 100 pF load; you can obtain shorter rise times by adding additional pullup resistors between the output and Vcc for that port.

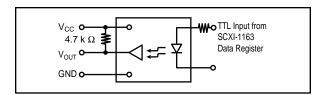


Figure 3-5. SCXI-1163 Digital Output Diagram

Note: It is important to notice that this module has no access to the analog backplane; this protects the backplane from faults when high voltages are available at the module outputs.

| Bank | Channels | Front Connector Pins |
|------|--------------------------|------------------------------|
| 0 | 0, 1, 2, 3, Vcc, GND | B30, A30, B29, A29, C30, C29 |
| 1 | 4, 5, 6, 7, Vcc, GND | B26, A26, B25, A25, C26, C25 |
| 2 | 8, 9, 10, 11, Vcc, GND | B22, A22, B21, A21, C22, C21 |
| 3 | 12, 13, 14, 15, Vcc, GND | B18, A18, B17, A17, C18, C17 |
| 4 | 16, 17, 18, 19, Vcc, GND | A13, B13, A14, B14, C13, C14 |
| 5 | 20, 21, 22, 23, Vcc, GND | A9, B9, A10, B10, C9, C10 |
| 6 | 24, 25, 26, 27, Vcc, GND | A5, B5, A6, B6, C5, C6 |
| 7 | 28, 29, 30, 31, Vcc, GND | A1, B1, A2, B2, C1, C2 |

Table 3-2. Channel and Bank Assignments

Chapter 4 Register Descriptions

This chapter describes in detail the SCXI-1163 Address Handler, the Module ID Register, the Data Register, the Status registers, and the SCXI-1000/1001 Slot 0 registers.

Note: If you plan to use a programming software package such as NI-DAQ, LabWindows, or LabVIEW with your SCXI-1163 board, you do not need to read this chapter.

Register Description

Register Description Format

This register description chapter discusses each of the SCXI-1163 registers and the Slot 0 registers. A detailed bit description of each register is given. The individual register description gives the type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB shown on the left (bit 31 for a 32-bit register, bit 15 for a 16-bit register, bit 7 for an 8-bit register), and the LSB shown on the right (bit 0). A rectangle is used to represent each bit. Each bit is labeled with a name inside its rectangle. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic). The Module ID register has a unique format and is described in the *Module ID Register* section.

In many of the registers, several bits are labeled with an X, indicating don't care bits. When you write to a register, you may set or clear these bits without effect.

SCXI-1163 Registers

The SCXI-1163 has an address handler that chooses one of the following five registers. The Address Handler is a write-only register that contains the address of the register to be read from or written to. The Module ID Register is a 4-byte read-only register that contains the Module ID number of the SCXI-1163. The Data Register is a 32-bit write-only register that controls the output states on the SCXI-1163. The Status registers are 1-bit registers that indicate the mode of operation of the module–serial, parallel, or serial override. The Parking Register is a dummy register located at address FFFF.

Register Descriptions Chapter 4

Address Handler

You must write to the Address Handler at the beginning of each write to or read from the SCXI-1163. Write the address of the register of interest to this handler, which in turn enables the register. This register is two bytes long and contains the address of the register to be read from or written to. The Address Handler is selected when SS* is asserted low and D*/A indicates an address transfer (D*/A is high). At this time, the address is shifted in the Address Handler register, MSB first. Table 4-1 lists the register addresses.

| Address (Hexadecimal) | Register |
|--|---|
| 0000 0001 0002 0003 0006 FFFF | Module ID Register Data Register A (enables serial override) Primary Mode Register Output Mode Register Data Register B (disables serial override) Parking Register |

Table 4-1. SCXI-1163 Register Addresses

After you have finished writing, the D^*/A line goes low, indicating a data transfer to a register. This enables the Address Handler output and selects the appropriate register.

You should select the Parking Register (write address FFFF to the Address Handler) after communication with one of the other registers. This increases the noise immunity of the module when the module is in its quiescent state.

After you select the Parking Register, SS* should be released high, which deselects the module and latches all of the data.

At reset or at power up, the Address Handler content is cleared.

Chapter 4 Register Descriptions

Module ID Register

The Module ID register contains the 4-byte module ID code for the SCXI-1163. This code number is read on the MISO line whenever the Module ID register is accessed. The bytes appear least significant byte first. Within each byte, data is sent out MSB first. Additional data transfers result in all zeros being sent on the MISO line. The Module ID register is reinitialized to its original value each time the module is deselected, reset, or powered up. The Module ID Register address is hexadecimal 0000.

Type: Read-only

Word Size: 4-byte

Bit Map:

| D4- 0 | | | | | | | |
|-------------|---|---|---|---|---|---|---|
| Byte 0 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | 4 | | | 1 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| | | | | | | | |
| Byte 1 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | |
| Byte 2 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | |
| Byte 3 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Register Descriptions Chapter 4

Data Register

The Data Register contains 32 bits that control the state of each output of the SCXI-1163. Whenever the Data Register is selected by the Address Handler, the Data Register shifts in the data present on the MOSI line, bit 31 first, and then latches the data when deselected. At power up or at reset, the Data Register contains all logic highs. The Data Register has two addresses—hexadecimal 0001 and 0006. After a write to address 0001, the Data Register drives the outputs regardless of the jumper-set primary mode of operation (either serial or parallel). After a write to address 0006, the Data Register drives the outputs only if the primary mode of operation is set to serial; if the primary mode is set to parallel, the outputs are driven to the logic levels seen at the rear connector.

Type: Write-only

Word Size: 32-bit

Bit Map:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| OUT(31) | OUT(30) | OUT(29) | OUT(28) | OUT(27) | OUT(26) | OUT(25) | OUT(24) |
| | | | | | | | - |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUT(23) | OUT(22) | OUT(21) | OUT(20) | OUT(19) | OUT(18) | OUT(17) | OUT(16) |
| | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OUT(15) | OUT(14) | OUT(13) | OUT(12) | OUT(11) | OUT(10) | OUT(9) | OUT(8) |
| | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT(7) | OUT(6) | OUT(5) | OUT(4) | OUT(3) | OUT(2) | OUT(1) | OUT(0) |

| Bit | Name | Description |
|------|----------|--|
| 31-0 | OUT<310> | Output (31 through 0) – Determine the state of the outputs. If set to 0, the outputs are driven low. If set to 1, the outputs are pulled high. |

Chapter 4 Register Descriptions

Status Registers

The Status Registers are 1-bit read-only registers that indicate the primary (jumper-set) mode of operation and the mode of operation currently driving the outputs. The register at address 0002 holds the Primary Mode Status; the register at address 0003 holds the Output Mode Status.

Primary Mode Status Register

A 1 indicates that the primary mode of operation is set for parallel writes, while a 0 indicates that the primary mode of operation is set for serial writes.

Output Mode Status Register

A 1 indicates that the outputs are being set by the data contents of the data register, while a 0 indicates that the outputs are being set in parallel by the levels seen at the rear connector.

Register Descriptions Chapter 4

Parking Register

This register is a dummy register that you should select after the end of a read or write operation. Selecting the Parking Register places the module in a state insensitive to noise and to electrostatic discharge (ESD), which may corrupt the Data Register content and cause the outputs to change state.

Select the Parking Register by writing FFFF (hexadecimal) to the Address Handler.

Chapter 4 Register Descriptions

Slot 0 Register Descriptions

Slot 0 has three registers—the FIFO Register, the Hardscan Register, and the Slot-Select Register. Only the Slot-Select Register is relevant to this module. The Slot-Select Register is a 16-bit write-only register that determines with which slot the data acquisition board speaks when SLOT0SEL* is released high. With the SCXI-1001 chassis, the Slot-Select Register also determines in which chassis the desired slot is. Write to the Slot-Select Register using the SLOT0SEL* line. Maintain software copies of the Slot-Select Register.

If you are using multiple chassis, it is important to understand the architecture of the Slot-Select Register. Although each chassis has its own physical Slot-Select Register, all are written to at the same time. The jumper settings in Slot 0 of a chassis determine with which chassis number Slot 0 is identified. From the software perspective, only one Slot-Select Register exists in a system composed of multiple chassis.

Register Descriptions Chapter 4

Slot-Select Register

The Slot-Select Register contains 16 bits that determine which module in which chassis is enabled for communication when the SLOT0SEL* line is high. An SCXI-1000 chassis selects the appropriate module in its chassis, regardless of the chassis number written. The Slot-Select Register shifts in the data present on the MOSI line, bit 15 first, when SLOT0SEL* is low.

Type: Write-only

Word Size: 16-bit

Bit Map:

| _ | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|------|------|------|------|-----|-----|-----|------|
| | X | X | X | X | X | X | X | CHS4 |
| | | | | | | | | |
| _ | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | CHS3 | CHS2 | CHS1 | CHS0 | SL3 | SL2 | SL1 | SL0 |

| Bit | Name | Description |
|------|---------|---|
| 15-9 | X | Don't care bits – Unused. |
| 8-4 | CHS<40> | Chassis Bit 4 through 0 – Determine which chassis is selected. On the SCXI-1000 chassis, these are don't care bits. |
| 3-0 | SL<30> | Slot Bit 3 through 0 – Determine which slot in the selected chassis is selected. |

Chapter 5 Programming

This chapter contains a functional programming description of the SCXI-1163 and Slot 0.

Note: If you plan to use a programming software package such as NI-DAQ, LabWindows, or LabVIEW with your SCXI-1163 board, you do not need to read this chapter.

Programming Considerations

Programming the SCXI-1163 involves writing to the Data Register. Programming the data acquisition boards involves writes to their registers. See your data acquisition board user manual for more information. The programming instructions list the sequence of steps to take. The instructions are language independent; that is, they instruct you to write a value to a given register without presenting the actual code.

Notation

For the bit patterns to be written, the following symbols are used:

- 0 binary zero
- 1 binary one
- X don't care; either zero or one may be written

The bit patterns are presented MSB first, left to right.

Register Writes

This section describes how to write to the Data Register including the procedure for writing to the Slot-Select Register to select the appropriate slot. For timing specifics, refer to the *Timing Requirements and Communication Protocol* section in Chapter 2, *Configuration and Installation*. Table 5-1 lists the rear signal connector pin equivalences to the different National Instruments data acquisition boards. See also Appendix E, *SCXI-1163 Cabling*. The Data Register is a write-only register.

The different bits in this register control independent output channels. There are times when you may want to set a specific channel or channels without affecting the remaining channels. However, a write to the Data Register affects all channels simultaneously. You cannot read the register to determine which channels have been set or reset in the past; therefore, you should maintain a software copy of the channel states. You can then read the software copy to determine the status of the channels. To change the state of a single channel without disturbing the remaining channels, change the bit that controls the channel of interest, set all other bits to the states last written to them, and rewrite to the Data Register.

Programming Chapter 5

Table 5-1. SCXIbus to SCXI-1163 Rear Signal Connector to Data Acquisition Board Pin Equivalences

| SCXIbus Line | SCXI-1163 Rear Signal Connector | MIO Boards | Lab-NB/Lab-PC/ Lab-PC+/Lab-LC | PC-LPM-16 | DIO-24 | 96-OIQ | DIO-32F |
|--------------|------------------------------------|------------|----------------------------------|-----------|--------|--------|---------|
| MOSI | SERDATIN | ADIO0 | PB4 | DOUT4 | PB3 | APB3 | DIOB3 |
| D*/A | DAQD*/A | ADIO1 | PB5 | DOUT5 | PB2 | APB2 | DIOB2 |
| INTR* | SLOT0SEL* | ADIO2 | PB6 | DOUT6 | PB1 | APB1 | DIOB1 |
| SPICLK | SERCLK | EXTSTROBE* | PB7 | DOUT7 | PB0 | APB0 | DIOB0 |
| MISO | SERDATOUT | BDIO0 | PC1 | DIN6 | PA0 | APA0 | DIOA0 |

Register Selection and Write Procedure

1. Select the slot of the module to be written to. Initial conditions:

SERDATIN = X. DAQD*/A = 1. SLOT0SEL* = 1. SERCLK = 1.

- 2. Clear SLOTOSEL* to 0. This deasserts all SS* lines to all modules in all chassis.
- 3. For each bit, starting with the MSB (bit 15), do the following:
 - a. Set SERDATIN = bit to be sent. These bits are the data that is written to the Slot-Select Register.
 - b. Clear SERCLK to 0.
 - c. Set SERCLK to 1. This rising edge clocks the data. If you are using an MIO-16 board, writing to the EXTSTROBE* register pulses EXTSTROBE* low and then high, accomplishing steps 3b and 3c.
- 4. Set SLOTOSEL* to 1. This asserts the SS* line of the module whose slot number was written to Slot 0. If you are using multiple chassis, only the appropriate slot in the chassis whose address corresponds to the written chassis number is automatically selected. When no communication is taking place between the data acquisition board and any modules, write zero to the Slot-Select Register to ensure that no accidental writes occur.

Chapter 5 Programming

5. If you are writing to a Data Register, you must first write address 0001 (hexadecimal) or address 0006 (hexadecimal) to the Address Handler. See Chapter 4, *Register Descriptions*, for a discussion on the uses of the two addresses. Then follow these steps:

- a. Establish the desired SERDATIN level corresponding to this bit.
- b. Clear SERCLK to 0.
- c. Set SERCLK to 1 (clock the data). If you are using an MIO-16 board, writing to the EXTSTROBE* register pulses EXTSTROBE* low and then high, accomplishing steps 5b and 5c.
- d. After you have written all the address bits, clear DAQD*/A to 0. This selects the Data Register, and the data on the MOSI line is written to the Data Register.
- 6. For each bit to be written to the Data Register:
 - a. Establish the desired SERDATIN level corresponding to this bit.
 - b. Clear SERCLK to 0.
 - c. Set SERCLK to 1 (clock the data). If you are using an MIO-16 board, writing to the EXTSTROBE* register pulses EXTSTROBE* low and then high, accomplishing steps 6b and 6c.
 - d. After clocking the last data bit, if you do not want to write to or read another register, write hexadecimal address FFFF to the Address Handler to increase the noise immunity of the module when it is in the quiescent state. This also latches the data into the Data Register. Selecting another register also latches the data in the Data Register.
- 7. Pull SLOTOSEL* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 8. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register. If you are selecting another slot, repeat the procedure starting at step 3.

For a timing illustration of a Data Register write, see Figure 2-8, *Data Register Write Timing Diagram*.

Initialization

The SCXI-1163 powers up with its Data Register set to logic ones and with the output mode of operation the same as the jumper-set primary mode of operation. If you reset the chassis, the Data Register resets to logic ones, and the output mode reverts to the primary mode of operation.

Programming Chapter 5

Examples

This section describes how to program the SCXI-1163, either alone or in conjunction with other modules.

The following examples are intended to aid your understanding of module and Slot 0 programming. It will be helpful to refer to the bit descriptions for the *Data Register*, *Status Register*, and *Address Handler* in Chapter 4, *Register Descriptions*.

Example 1

You want to set all the outputs to their logic high state on an SCXI-1163 in Slot 1 of an SCXI-1000 chassis. The SCXI-1163 is directly cabled to a data acquisition board and has the primary mode of operation set to serial.

The programming steps are as follows:

Example 2

An SCXI-1000 chassis has four SCXI-1163 modules in Slots 1, 2, 3, and 4. The SCXI-1163 in Slot 4 is cabled to the data acquisition board and has the primary mode set to serial. The SCXI-1163 in Slot 3 is not cabled to a data acquisition board and has the primary mode set to parallel. You want to set the following channels to their logic low states and leave all the other channels in their logic high states. The channels of interest in each slot are as follows:

- Channel 3 on the SCXI-1163 in Slot 1
- Channels 0 through 2 on the SCXI-1163 in Slot 4
- Channels 10, 7, 5, and 3 on the SCXI-1163 in Slot 3

The programming steps are as follows:

- 1. Following the procedure given in the *Register Writes* section of this chapter, write 11111111 11111111 11111111 11110111 to the Data Register of the SCXI-1163 in Slot 1.
- 2. Following the procedure given in the *Register Writes* section of this chapter, write 11111111 111111111 11111111 111111000 to the Data Register of the SCXI-1163 in Slot 4.
- 3. Following the procedure given in the *Register Writes* section of this chapter, write 11111111 11111111 11111011 010101111 to the Data Register of the SCXI-1163 in Slot 3. Since this module is jumpered for a parallel mode of primary operation, the Data Register *must* be written to via address 0001 (hex) to ensure that the output mode is serial and therefore that the Data Register drives the outputs.

Chapter 5 Programming

Example 3

You have a multiple-chassis system with an SCXI-1163 in Slots 4 and 8 of Chassis 1, and another SCXI-1163 in Slot 11 of Chassis 2. The SCXI-1163 in Slot 8 of Chassis 1 is configured for a primary mode of operation of parallel, but you have been writing to it in serial by using address 0001 to access the Data Register. The other two modules have their primary modes of operation set to serial. You want to do the following:

- 1. In Chassis 1, Slot 4, set the outputs to their high states on channels 1, 5, and 18, leaving all other channels in their low states.
- 2. In Chassis 1, Slot 8, return control of the outputs to parallel control via the rear connector.
- 3. In Chassis 2, set the outputs to their low states on channels 0 through 7 and on 23, leaving all other channels in their high states.

Leave all other channels unchanged.

Assuming that the modules are cabled correctly and jumpers W5 and W1 are set correctly, do the following:

- 1. Select Chassis 1, Slot 4 as described in the *Register Writes* section of this chapter.
- 2. Following the procedure given in the *Register Writes* section of this chapter, write 00000000 00000100 00000000 00100010.
- 3. Select Chassis 1, Slot 8 as described in the *Register Writes* section of this chapter.
- 4. Following the procedure given in the *Register Writes* section of this chapter, select address 0006 and write anything (XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX) to the Data Register. Using address 0006 will return control of the outputs to the rear connector in parallel, so the pattern written to the Data Register becomes irrelevant.
- 3. Select Chassis 2, Slot 11 as described in the *Register Writes* section of this chapter.
- 4. Following the procedure given in the *Register Writes* section of this chapter, write 11111111 01111111 11111111 00000000.

Appendix A Specifications

This appendix lists the specifications for the SCXI-1163. These are typical at 25° C and 50% humidity unless otherwise stated. The operating temperature range is 0° to 50° C.

Digital Outputs

Power requirements (per port)

Supply voltage $+5 \text{ V} \pm 0.5 \text{ V}$

+7 V absolute maximum

Supply current 60 mA/port typical

80 mA/port maximum

Outputs Open-collector digital outputs with 4.7 k Ω pullups

Logic low output voltage

(I_{out} = 12 mA) 0.4 V typical 0.6 V maximum

Output current (outputs low) 15 mA maximum

Isolation Port to port and port to ground

Breakdown 1,900 Vrms maximum Working 450 Vrms maximum

Maximum speed

Propagation delay (parallel mode) 100 nsec Rise time¹ (into 100 pF) 1 µsec

Serial data rate

Measured using NI-DAQ software

on a 486-50 computer

Measured using NI-DAQ software

on a 386-33 computer 350 writes/sec

Common-mode rejection 500 V/µsec typical

100 V/µsec minimum

700 writes/sec

Physical

Dimensions 1.2 by 6.8 by 8.0 in.

Connectors 50-pin male ribbon-cable rear connector

48-pin DIN C male front connector (48-screw terminal adapter available)

¹You can add pullup resistors to obtain faster rise times. Be aware, however, that adding pullup resistors accordingly increases the current that the output uses.

Specifications Appendix A

Operating Environment

Temperature 0° to 50° C

Relative humidity 5% to 90% at 35° C

Storage Environment

Temperature -55° to 150° C

Relative humidity 5% to 90% noncondensing

Appendix B Rear Signal Connector

This appendix describes the pinout and signal names for the SCXI-1163 50-pin rear signal connector, including a description of each connection.

Figure B-1A shows the pin assignments for the SCXI-1163 rear signal connector configured for serial communication. Figure B-1B shows the pin assignments for the rear signal connector configured for parallel communication.

Rear Signal Connector Appendix B

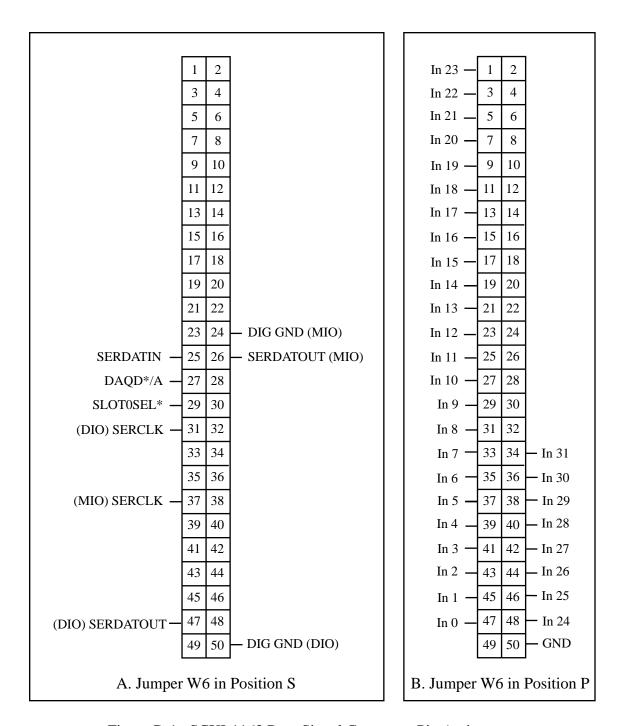


Figure B-1. SCXI-1163 Rear Signal Connector Pin Assignment

Appendix B Rear Signal Connector

Rear Signal Connector Signal Descriptions, Serial Configuration

| Pin | Signal Name | Description |
|----------|-------------|---|
| 24 or 50 | DIG GND | Digital Ground – Supplies the reference for data acquisition board digital signals and is tied to the module digital ground. Pin 50 is for DIO-type boards. Pin 24 is for MIO-type boards. Jumper W3 selects the pin. |
| 25 | SERDATIN | Serial Data In – Taps into the SCXIbus MOSI line to provide serial input data to a module or Slot 0. |
| 26 or 47 | SERDATOUT | Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module. Pin 47 is for DIO-type boards. Pin 26 is for MIO-type boards. Jumper W5 selects the pin. |
| 27 | DAQD*/A | Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information. |
| 29 | SLOT0SEL* | Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is sent to a module or to Slot 0. |
| 31 or 37 | SERCLK | Serial Clock – Taps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines. Pin 31 is for DIO-type boards. Pin 37 is for MIO-type boards. Jumper W2 selects the pin. |

^{*} Indicates active low.

All other pins are not connected.

See the *Timing Requirements and Communication Protocol* section in Chapter 2, *Configuration and Installation*, for more detailed information on timing.

Rear Signal Connector Signal Descriptions, Parallel Configuration

| Pin | Signal Name | Description |
|--|-------------|--|
| 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23, 21, 19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 48, 46, 44, 42, 40, 38, 36, 34 | In <031> | Digital Inputs – The logic levels at these inputs determine the output states. |
| 50 | GND | Ground – Supplies ground reference for the parallel inputs. |

Rear Signal Connector Appendix B

All other pins are not connected.

See the *Timing Requirements and Communication Protocol* section in Chapter 2, *Configuration and Installation*, for more detailed information on timing.

Appendix C SCXIbus Connector

This appendix describes the pinout and signal names for the SCXI-1163 SCXIbus connector, including a description of each connection.

Figure C-1 shows the pin assignments for the SCXI-1163 SCXIbus connector.

SCXIbus Connector Appendix C

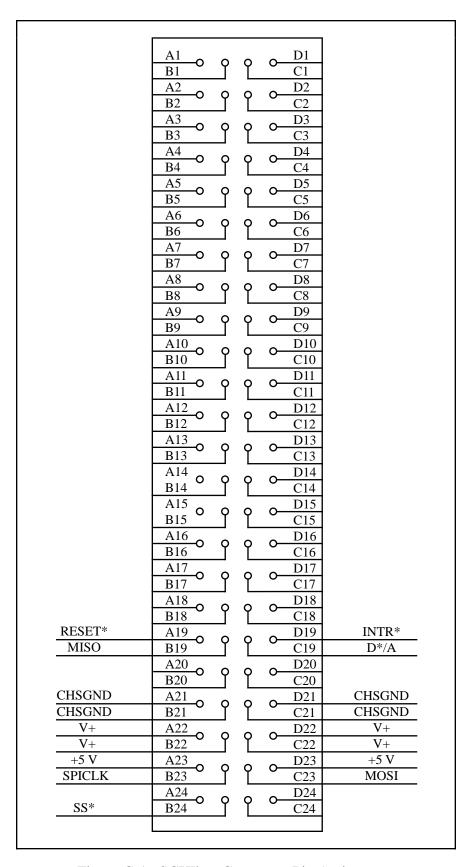


Figure C-1. SCXIbus Connector Pin Assignment

Appendix C SCXIbus Connector

SCXIbus Connector Signal Descriptions

| Pin | Signal Name | Description |
|-----------------------|-------------|--|
| A19 | RESET* | Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input. |
| B19 | MISO | Master-In-Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O. |
| C19 | D*/A | Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O. |
| D19 | INTR* | Interrupt – Active low. Causes data that is on MOSI to be written to the Slot 0 Slot-Select Register. Open collector. Output. |
| A21, B21, C21, D21 | CHSGND | Chassis Ground – Digital and analog ground reference. |
| A22, B22, C22, D22 | V+ | Positive Analog Supply – +18.5 to +25 V. |
| A23, D23 | +5 V | +5 VDC Source – Digital power supply. |
| B23 | SPICLK | Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O. |
| C23 | MOSI | Master-Out-Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O. |
| B24 | SS* | Slot Select – When low, enables module communications over the SCXIbus. Totem pole. Input. |

^{*} Indicates active low.

All other pins are not connected.

Further information is given in Chapter 3, *Theory of Operation*.

Appendix D SCXI-1163 Front Connector

This appendix describes the pinout and signal names for the SCXI-1163 front connector, including a description of each connection.

Figure D-1 shows the pin assignments for the SCXI-1163 front connector.

SCXI-1163 Front Connector Appendix D

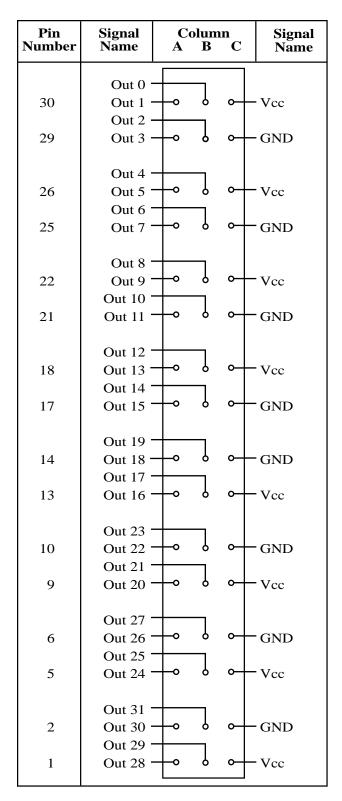


Figure D-1. SCXI-1163 Front Connector Pin Assignment

Front Connector Signal Descriptions

| Pin | Signal Name | Description |
|-----------------------|-------------|----------------|
| B30, A30, B29, A29 | Out<03> | Port 0 outputs |
| C30 | Vcc | Port 0 power |
| C29 | GND | Port 0 ground |
| B26, A26, B25, A25 | Out<47> | Port 1 outputs |
| C26 | Vcc | Port 1 power |
| C25 | GND | Port 1 ground |
| B22, A22, B21, A21 | Out<811> | Port 2 outputs |
| C22 | Vcc | Port 2 power |
| C21 | GND | Port 2 ground |
| B18, A18, B17, A17 | Out<1215> | Port 3 outputs |
| C18 | Vcc | Port 3 power |
| C17 | GND | Port 3 ground |
| A13, B13, A14, B14 | Out<1619> | Port 4 outputs |
| C14 | GND | Port 4 ground |
| C13 | Vcc | Port 4 power |
| A9, B9, A10, B10 | Out<2023> | Port 5 outputs |
| C10 | GND | Port 5 ground |
| C9 | Vcc | Port 5 power |
| A5, B5, A6, B6 | Out<2427> | Port 6 outputs |
| C6 | GND | Port 6 ground |
| C5 | Vcc | Port 6 power |

SCXI-1163 Front Connector Appendix D

| Pin | Signal Name | Description (continued) |
|-------------------|-------------|--------------------------------|
| A1, B1, A2, B2 | Out<2831> | Port 7 outputs |
| C2 | GND | Port 7 ground |
| C1 | Vcc | Port 7 power |

Further information is given in Chapter 2, Configuration and Installation.

This appendix describes how to use and install the hardware accessories for the SCXI-1163:

- SCXI-1340 cable assembly
- SCXI-1341 Lab-NB, Lab-PC, and Lab-PC+ cable assembly
- SCXI-1344 Lab-LC cable assembly
- SCXI-1342 PC-LPM-16 cable assembly
- SCXI-1348 DIO-32 cable assembly
- SCXI-1180 feedthrough panel
- SCXI-1302 50-pin terminal block
- SCXI-1351 one-slot cable extender
- SCXI-1350 multichassis adapter
- SCXI-1343 screw terminal adapter

SCXI-1340 Cable Assembly

The SCXI-1340 cable assembly connects an MIO-16 or DIO-24 board to an SCXI-1163 module. The SCXI-1340 consists of a mounting bracket at one end and a 50-conductor ribbon cable that has a 50-pin female connector at the other end. This female connector attaches to the I/O connector of the data acquisition board. Attached to the mounting bracket is a 50-pin female mounting bracket connector that connects to the rear signal connector of the module. A male breakout connector is near the mounting bracket on the ribbon cable. You can use this male breakout connector to extend the signals of the MIO-16 or DIO-24 board to an SCXI-1180 feedthrough panel or an SCXI-1181 breadboard module. All 50 pins from the MIO-16 or DIO-24 board go straight to the rear signal connector. You can use a standard 50-pin ribbon cable in lieu of the SCXI-1340 cable assembly.

The SCXI-1340 has the following advantages over the ribbon cable:

- The SCXI-1340 provides strain relief so that you cannot accidentally disconnect the cable.
- The SCXI-1340 includes a mounting bracket that mounts to the chassis so that you can remove and reinsert the module without explicitly removing the cable from the back of the chassis. This is especially useful when the SCXI chassis is rack mounted, making rear access difficult.

• The SCXI-1340 has an extra male breakout connector for use with the SCXI-1180 feedthrough panel or additional modules or breadboards that need a direct connection to the MIO-16 or DIO-24 board.

• The SCXI-1340 rear panel gives the module and the chassis both mechanical and electrical shielding.

Table E-1 lists the pin equivalences of the MIO-16 and DIO-24 boards and the SCXI-1163.

Table E-1. SCXI-1163 and Board Pinout Equivalences

| Pin | SCXI-1163 Rear Signal | Connector | MIO-16 Board Equivalent | DIO-24 Board Equivalent |
|---|----------------------------------|---|----------------------------|---|
| | Serial | Parallel | | |
| 1 3 5 7 9 11 13 15 17 19 21 23 24 | DIG GND (MIO) | In (23) In (22) In (21) In (20) In (19) In (18) In (17) In (16) In (15) In (14) In (13) In (12) | DIG GND | PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0 PB7 PB6 PB5 PB4 |
| 25 26 | SERDATIN SERDATOUT (MIO) | In (11) | ADIO0 BDIO0 | PB3 |
| 27 | DAQD*/A | In (10) | ADIO1 | PB2 |
| 29 | SLOTOSEL* | In (9) | ADIO2 | PB1 |
| 31 33 | SERCLK (DIO) | In (8) In (7) | | PB0 PA7 |
| 35 | | In (7) In (6) | | PA6 |
| 37 39 41 43 45 | SERCLK (MIO) | In (5) In (4) In (3) In (2) In (1) | EXTSTROBE* | PA5 PA4 PA3 PA2 PA1 |
| 47 50 | SERDATOUT (DIO) DIG GND (DIO) | In (0) GND | | PA0 DIG GND |

No other pins are connected on the SCXI-1163.

SCXI-1340 Installation

Follow these steps to install the SCXI-1340:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Plug the mounting bracket connector onto the module rear signal connector (see Figure E-1). An alignment tab on the bracket enters the upper board guide of the chassis.
- 4. Screw the mounting bracket to the threaded strips in the rear of the chassis.
- 5. Connect the loose end of the cable assembly to the MIO-16 or DIO-24 board rear signal connector.

Check the installation.

After step 1, the order of these steps is not critical; however, it is easier to locate the correct position for the mounting bracket with a module installed in the chassis. If you are attaching a cable to the breakout connector, installation is easiest if you attach the second cable before installing the SCXI-1340.

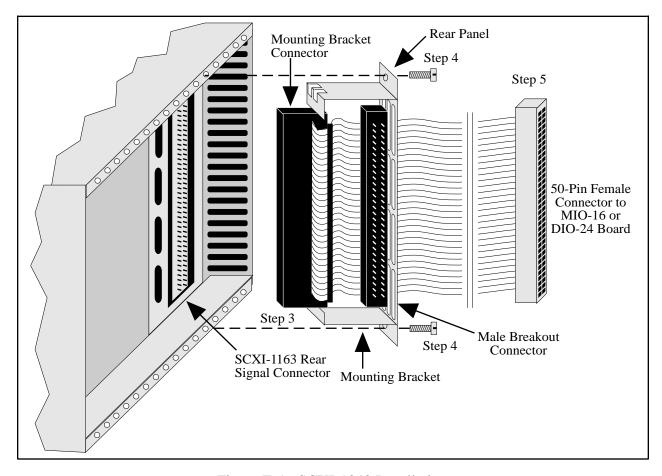


Figure E-1. SCXI-1340 Installation

SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ and SCXI-1344 Lab-LC Cable Assembly

The SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ cable assembly connects a Lab-NB, Lab-PC, or Lab-PC+ board to an SCXI-1163 module. The SCXI-1344 Lab-LC cable assembly connects a Lab-LC board to an SCXI-1163 module. The SCXI-1341 and SCXI-1344 cable assemblies consist of two pieces—an adapter board and a 50-conductor ribbon cable that connects the Lab board to the rear connector of the adapter board. The adapter board converts the signals from the Lab board I/O connector to a format compatible with the SCXI-1163 rear signal connector pinout at the front connector of the SCXI-1341 or SCXI-1344. The adapter board also has an additional male breakout connector that provides the unmodified Lab board signals for use with an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board gives the Lab boards full access to the digital control lines. The position of jumper W1 on the SCXI-1341 and SCXI-1344 is irrelevant because the SCXI-1163 does not use jumper W1. Table E-2 lists the SCXI-1341 and SCXI-1344 pin translations.

Table E-2. SCXI-1341 and SCXI-1344 Pin Translations

| Lab Board Pin | Lab Board Signal | SCXI-1163 Pin | SCXI-1163 Signal |
|---------------|------------------|---------------|------------------|
| 1 | ACH0 | 3 | No Connect |
| 2 | ACH1 | 5 | No Connect |
| 3 | ACH2 | 7 | No Connect |
| 4 5 | ACH3 | 9 | No Connect |
| 5 | ACH4 | 11 | No Connect |
| 6 | ACH5 | 13 | No Connect |
| 7 | ACH6 | 15 | No Connect |
| 8 9 | ACH7 | 17 | No Connect |
| 9 | AIGND | 1-2 | No Connect |
| 10 | DAC0OUT | 20 | No Connect |
| 11 | AOGND | 23 | No Connect |
| 12 | DAC1OUT | 21 | No Connect |
| 13, 50 | DGND | 24 | DIG GND |
| 26 | PB4 | 25 | SERDATIN |
| 27 | PB5 | 27 | DAQD*/A |
| 28 | PB6 | 29 | SLOT0SEL* |
| 29 | PB7 | 37 | SERCLK |
| 31 | PC1 | 26 | SERDATOUT |
| 32 | PC2 | 28 | No Connect |
| 40 | EXTCONV* | 36 | No Connect |
| 43 | OUTB1 | 46 | No Connect |
| 49 | +5 V | 34-35 | No Connect |

All other pins of the Lab board pinout are not sent to the SCXI-1163 rear signal connector.

SCXI-1341 and SCXI-1344 Installation

Follow these steps to install the SCXI-1341 or SCXI-1344:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Connect one end of the ribbon cable to the adapter board rear connector. This is the 50-pin connector of the SCXI-1344 cable.
- 4. Plug the adapter board front connector to the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.
- 6. For an SCXI-1341, connect the loose end of the ribbon cable to the Lab-NB, Lab-PC, or Lab-PC+ I/O connector. For an SCXI-1344, connect the two 26-pin connectors to the Lab-LC board according to the instructions given in the *Installation* section of Chapter 2, *Configuration and Installation*, of the *Lab-LC User Manual*.

Check the installation.

SCXI-1342 PC-LPM-16 Cable Assembly

The SCXI-1342 PC-LPM-16 cable assembly connects a PC-LPM-16 board to an SCXI-1163 module. The SCXI-1342 cable assembly consists of two pieces—an adapter board and a 50-conductor ribbon cable that connects the PC-LPM-16 board to the adapter board. The adapter board converts the signals from the PC-LPM-16 I/O connector to a format compatible with the SCXI-1163 rear signal connector pinout. The adapter board also has an additional male breakout connector that provides the unmodified PC-LPM-16 signals for use with an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board gives the PC-LPM-16 full access to the digital control lines. The position of jumper W1 on the SCXI-1342 is irrelevant because the SCXI-1163 does not use jumper W1. Table E-3 lists the SCXI-1342 pin translations.

Table E-3. SCXI-1342 Pin Translations

| PC-LPM-16 Pin | PC-LPM-16 Signal | Rear Signal Connector Pin | SCXI-1163 Use |
|---------------|------------------|------------------------------|---------------|
| 1-2 | AIGND | 1-2 | No Connect |
| 3 | ACH0 | 3 | No Connect |
| 4 | ACH8 | 4 | No Connect |
| 5 | ACH1 | 5 | No Connect |
| 6 | ACH9 | 6 | No Connect |
| 7 | ACH2 | 7 | No Connect |
| 8 | ACH10 | 8 | No Connect |
| 9 | ACH3 | 9 | No Connect |
| 10 | ACH11 | 10 | No Connect |
| 11 | ACH4 | 11 | No Connect |
| 12 | ACH12 | 12 | No Connect |
| 13 | ACH5 | 13 | No Connect |
| 14 | ACH13 | 14 | No Connect |
| 15 | ACH6 | 15 | No Connect |
| 16 | ACH14 | 16 | No Connect |
| 17 | ACH7 | 17 | No Connect |
| 18 | ACH15 | 18 | No Connect |
| 19, 50 | DGND | 24 | DIG GND |
| 28 | DIN6 | 26 | SERDATOUT |
| 29 | DIN7 | 28 | No Connect |
| 34 | DOUT4 | 25 | SERDATIN |
| 35 | DOUT5 | 27 | DAQD*/A |
| 36 | DOUT6 | 29 | SLOT0SEL* |
| 37 | DOUT7 | 37 | SERCLK |
| 46 | OUT2 | 46 | No Connect |
| 49 | +5 V | 34-35 | No Connect |

All other pins of the PC-LPM-16 pinout are not sent to the SCXI-1163 rear signal connector.

SCXI-1342 Installation

Follow these steps to install the SCXI-1342:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module to which the SCXI-1342 will connect.
- 3. Connect one end of the ribbon cable to the adapter board rear connector.
- 4. Plug the adapter board front connector onto the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.
- 6. Connect the loose end of the ribbon cable to the PC-LPM-16 I/O connector.

DIO-96, AT-MIO-16D, and AT-MIO-64F-5 Board Connection

To use your SCXI-1163 with a DIO-96, AT-MIO-16D, or AT-MIO-64F-5 board, you need an NB5 cable. The NB5 cable is a ribbon cable with a 100-pin connector that mates with the data acquisition board rear signal connector. The other end of the cable is divided into two 50-pin connectors. Use positions 1 through 50 of the NB5 connector to control the SCXI-1163 and the SCXIbus via serial communication or to provide parallel inputs to the module. You can either connect the positions 1 through 50 connector of the NB5 cable directly to the SCXI-1163, or use an SCXI-1351 between the SCXI-1163 and the NB5 cable. The SCXI-1163 does not use positions 51 through 100 of the NB5 cable for serial communication; however, you can use those positions to provide parallel inputs to the module with the DIO-96 and AT-MIO-16D boards.

The SCXI-1351 has the following advantages over the ribbon cable:

- The SCXI-1351 provides strain relief so that you cannot accidentally disconnect the cable.
- The SCXI-1351 includes a mounting bracket that mounts to the chassis so that you can remove and reinsert the module without explicitly removing the cable from the back of the chassis. This is especially useful when the SCXI chassis is rack mounted, making rear access difficult.
- The SCXI-1351 has an extra female connector for use with the SCXI-1180 feedthrough panel or additional modules or breadboards that need a direct connection to the board.
- The SCXI-1351 rear panel gives the module and the chassis both mechanical and electrical shielding.

Table E-4 lists the pin equivalences of the DIO-96, AT-MIO-16D, and AT-MIO-64F-5 boards and the SCXI-1163.

Table E-4. SCXI-1163 and DIO-96, AT-MIO-16D, and AT-MIO-64F-5 Board Pinout Equivalences

| Pin | SCXI-1163 Rear Signal Connector | | DIO-96 Board Equivalent | AT-MIO-16D Board Equivalent | AT-MIO-64F-5 Board Equivalent |
|---|--|--|--|---|--|
| | Serial | Parallel | _ | | |
| 1 3 5 7 9 11 13 15 17 19 21 23 24 25 26 27 29 31 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 50 51 55 57 59 61 63 65 | SERDATIN DAQD*/A SLOT0SEL* SERCLK SERDATOUT DIG GND | In (23) In (22) In (21) In (20) In (19) In (18) In (17) In (16) In (15) In (14) In (13) In (12) In (11) In (10) In (9) In (8) In (7) In (31) In (6) In (30) In (5) In (29) In (4) In (28) In (27) In (29) In (4) In (26) In (1) In (26) In (1) In (26) In (1) In (27) In (26) In (1) In (27) In (29) In (21) In (20) In (21) In (20) In (19) In (18) In (17) In (16) | APC7 APC6 APC5 APC5 APC4 APC3 APC2 APC1 APC0 APB7 APB6 APB5 APB4 APB3 APB2 APB1 APB0 APA7 BPA7 APA6 BPA6 APA5 BPA5 APA4 BPA4 APA3 BPA3 APA2 BPA4 APA3 BPA1 APA0, BPA0 DIG GND CPC7 CPC6 CPC5 CPC4 CPC3 CPC2 CPC1 CPC0 | DIG GND ADIO0 BDIO0 ADIO1 ADIO2 EXSTROBE* PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0 | DIG GND ADIO0 BDIO0 ADIO1 ADIO2 EXSTROBE* |

(continues)

Table E-4. SCXI-1163 and DIO-96, AT-MIO-16D, and AT-MIO-64F-5 Board Pinout Equivalences (Continued)

| Pin | SCXI-1163 Re Connect | | DIO-96 Board Equivalent | AT-MIO-16D Board Equivalent | AT-MIO-64F-5 Board Equivalent |
|-----|-------------------------|----------|-------------------------------|-----------------------------------|-------------------------------------|
| | Serial | Parallel | | | |
| 67 | | In (15) | CPB7 | PB7 | |
| 69 | | In (14) | CPB6 | PB6 | |
| 71 | | In (13) | CPB5 | PB5 | |
| 73 | | In (12) | CPB4 | PB4 | |
| 75 | | In (11) | CPB3 | PB3 | |
| 77 | | In (10) | CPB2 | PB2 | |
| 79 | | In (9) | CPB1 | PB1 | |
| 81 | | In (8) | CPB0 | PB0 | |
| 83 | | In (7) | CPA7 | PA7 | |
| 84 | | In (31) | DPA7 | | |
| 85 | | In (6) | CPA6 | PA6 | |
| 86 | | In (30) | DPA6 | | |
| 87 | | In (5) | CPA5 | PA5 | |
| 88 | | In (29) | DPA5 | | |
| 89 | | In (4) | CPA4 | PA4 | |
| 90 | | In (28) | DPA4 | | |
| 91 | | In (3) | CPA3 | PA3 | |
| 92 | | In (27) | DPA3 | | |
| 93 | | In (2) | CPA2 | PA2 | |
| 94 | | In (26) | DPA2 | | |
| 95 | | In (1) | CPA1 | PA1 | |
| 96 | | In (25) | DPA1 | | |
| 97 | | In (0) | CPA0 | PA0 | |
| 98 | | In (24) | DPA0 | | |
| 100 | DIG GND | GND | DIG GND | GND | |

All other pins are not connected on the SCXI-1163.

SCXI-1351 and NB5 Cable Installation

Follow these steps to install the SCXI-1351:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Connect the positions 1 through 50 connector (or 51 through 100, as appropriate) of the NB5 cable to the male breakout connector on the SCXI-1351.
- 4. Plug the mounting bracket connector onto the module rear signal connector (see Figure E-2). An alignment tab on the bracket will enter the upper board guide of the chassis.
- 5. Screw the mounting bracket to the threaded strips in the rear of the chassis.
- 6. Connect the 100-pin connector of the NB5 cable to the board.

After step 1, the order of these steps is not critical; however, it is easier to locate the correct position for the mounting bracket with a module installed in the chassis. If you are attaching a cable to the female connector, installation is easiest if you attach the second cable before installing the SCXI-1351.

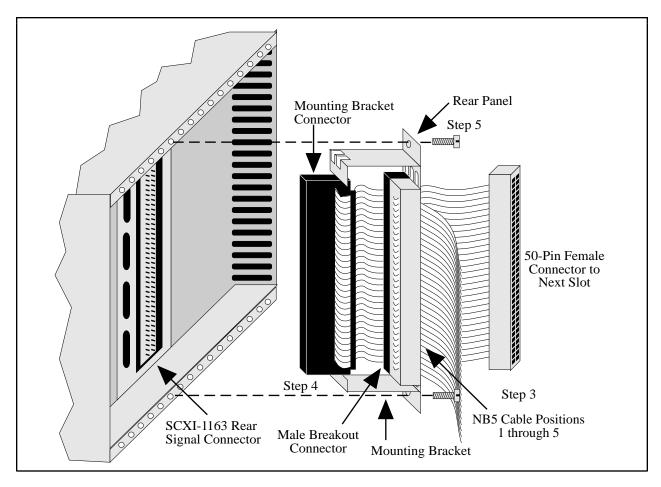


Figure E-2. SCXI-1351 and NB5 Cable Installation

SCXI-1348 DIO-32F Cable Assembly

The SCXI-1348 DIO-32F cable assembly connects a DIO-32F board to an SCXI-1163 module. The SCXI-1348 cable assembly consists of two pieces—an adapter board and a 50-conductor shielded ribbon cable that connects the DIO-32F board to the adapter board. The adapter board converts the signals from the DIO-32F I/O connector to a format compatible with the SCXI-1163 rear signal connector pinout. The adapter board also has an additional male breakout connector that provides the unmodified DIO-32F signals for use with an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board gives the DIO-32F full access to the digital control lines. Table E-5 lists the SCXI-1348 pin translations.

Table E-5. SCXI-1348 Pin Translations

| | DIO-32F Signal | Rear Signal Connector Pin | SCXI-1163 Use |
|----------------------------|----------------|------------------------------|-------------------|
| 1 | DIOD1 | 46 | In (25) |
| $\tilde{2}$ | DIOD4 | 40 | In (28) |
| - 3 | DIOD3 | 42 | In (27) |
| | DIOD0 | 48 | In (24) |
| 5 | DIOD6 | 36 | In (30) |
| 2 3 4 5 6 7 | DIOD7 | 34 | In (30) |
| | DIOD7 DIOD2 | 44 | In (26) |
| 8 | | 38 | |
| 9 | DIOD5 | | In (29) |
| | DIOC5 | 5 | In (21) |
| 10 | DIOC7 | 1 | In (23) |
| 11 | DIOC3 | 9 | In (19) |
| 12 | DIOC1 | 13 | In (17) |
| 13 | DIOC2 | 11 | In (18) |
| 14 | DIOC0 | 15 | In (16) |
| 15 | DIOC6 | 3 7 | In (22) |
| 16 | DIOC4 | | In (20) |
| 17, 19 | DIG GND | 2,4 | No Connect |
| 21, 23 | DIG GND | 6,8 | No Connect |
| 25, 26 | DIG GND | 10,12 | No Connect |
| 28, 30 | DIG GND | 14,16 | No Connect |
| 32, 34 | DIG GND | 50 | DIG GND |
| 18 | ACK2 | 26 | No Connect |
| 20 | IN2 | 28 | No Connect |
| $\frac{20}{22}$ | OUT2 | 30 | No Connect |
| 24 | REQ2 | 32 | No Connect |
| 27 | ACK1 | 18 | No Connect |
| 29 | IN1 | 20 | No Connect |
| 31 | OUT1 | 22 | No Connect |
| 33 | REQ1 | 24 | No Connect |
| 35 | DIOA4 | 39 | In (4) |
| 36 | DIOA4 DIOA6 | 35 | In (4) |
| 37 | DIOA0 DIOA0 | 47 | In (0), SERDATOUT |
| 38 | DIOA0 DIOA2 | 43 | 1 |
| 38 39 | DIOA2 DIOA1 | | In (2) |
| | _ | 45 | In (1) |
| 40 | DIOA3 | 41 | In (3) |
| 41 | DIOA7 | 33 | In (7) |
| 42 | DIOA5 | 37 | In (5) |
| 43 | DIOB5 | 21 | In (13) |
| 44 | DIOB2 | 27 | In (10), DAQD*/A |
| 45 | DIOB7 | 17 | In (15) |
| 46 | DIOB6 | 19 | In (14) |
| 47 | DIOB0 | 31 | In (8), SERCLK |
| 48 | DIOB3 | 25 | In (11), SERDATIN |
| 49 | DIOB4 | 23 | In (12) |
| 50 | DIOB1 | 29 | In (9), SLOT0SEL* |

SCXI-1348 Installation

Follow these steps to install the SCXI-1348:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module to which the SCXI-1348 will connect.
- 3. Connect one end of the ribbon cable to the adapter board rear connector.
- 4. Plug the adapter board front connector onto the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.
- 6. Connect the loose end of the ribbon cable to the DIO-32F I/O connector.

Check the installation.

SCXI-1180 Feedthrough Panel

The SCXI-1180 feedthrough panel provides front panel access to the signals of any data acquisition board that uses a 50-pin I/O connector. The SCXI-1180 consists of a front panel with a 50-pin male front panel connector that occupies one slot in the SCXI chassis, and a ribbon cable with a female rear connector and a male breakout connector. You can attach the rear connector to the male breakout connector of an SCXI-1340, SCXI-1341, SCXI-1342, SCXI-1344, or SCXI-1351 in the adjacent slot. The breakout connector further extends the cabling scheme. The front panel connector has the feedthrough connection. You can attach an SCXI-1302 terminal block to the front panel connector for simple screw terminal connections. A rear filler panel that shields and protects the interior of the SCXI chassis is also included.

SCXI-1180 Installation

Install the SCXI-1180 to the right of a slot that has an SCXI-1340, SCXI-1341, SCXI-1342, or SCXI-1344 cable assembly or an SCXI-1351 slot extender in its rear connector space.

Follow these steps to install the SCXI-1180:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Remove the front filler panel of the slot where you want to insert the SCXI-1180.
- 3. Thread the rear connector through the front of the chassis to the rear of the chassis. Attach the rear connector to the breakout connector of the adjacent cable assembly or slot extender, as shown in Figure E-3.
- 4. Screw in the rear panel to the threaded strip in the rear of the chassis.
- 5. Screw the front panel into the front threaded strip, as shown in Figure E-4.

Check the installation.

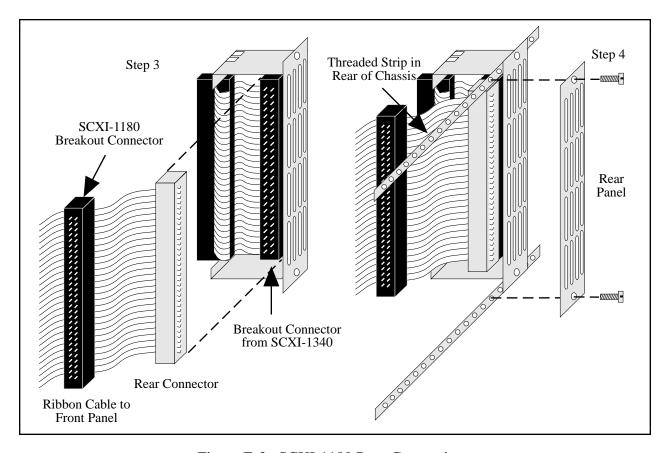


Figure E-3. SCXI-1180 Rear Connections

Note: If you are using the SCXI-1180 with an SCXI-1351 and an NB5 cable, connect the SCXI-1180 breakout connector to the female connector on the SCXI-1351. Place the SCXI-1180 to the *left* of the SCXI-1351 (looking at the front of the chassis).

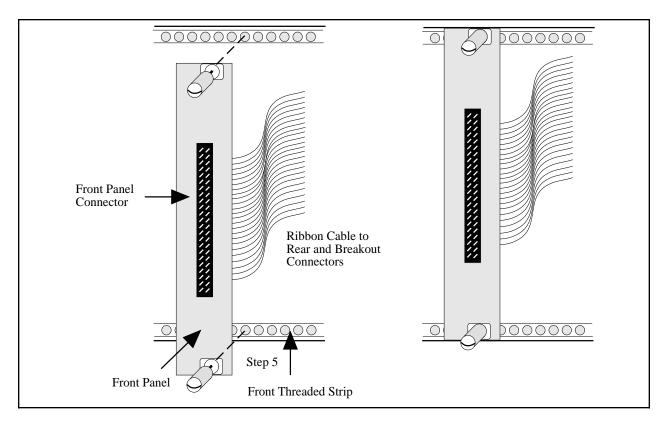


Figure E-4. SCXI-1180 Front Panel Installation

SCXI-1302 50-Pin Terminal Block

The SCXI-1302 terminal block has screw terminal connections for the 50-pin connector on the SCXI-1180 feedthrough panel.

SCXI-1302 Wiring Procedure

To wire the SCXI-1302 terminal block, you must remove the cover, connect all the wiring, and replace the cover. The procedure for this is as follows:

- 1. Unscrew the rear grounding screw on the back of the terminal block, as shown in Figure E-5.
- 2. With a flathead screwdriver, carefully pry the cover off the terminal block.
- 3. Insert each wire through the terminal block strain relief.
- 4. Connect the wires to the screw terminals.
- 5. Tighten the large strain relief screws to secure the wires.
- 6. Snap the cover back in place.
- 7. Reinsert the rear grounding screw. The terminal block is now ready to be connected to the front panel connector.

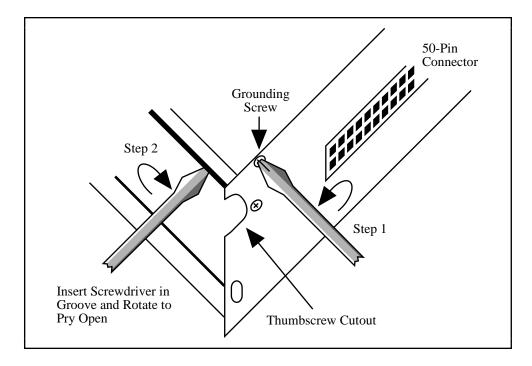


Figure E-5. Cover Removal

SCXI-1302 Installation

Follow these steps to install the SCXI-1302:

- 1. Install an SCXI-1180 feedthrough panel as described in the SCXI-1180 Installation section.
- 2. Wire the terminal block as previously described in the SCXI-1302 Wiring Procedure section.
- 3. Connect the SCXI-1302 terminal block to the front panel connector on the SCXI-1180 feedthrough panel. Be careful to fit the thumbscrews in the thumbscrew cutouts.
- 4. Tighten the top and bottom captive screws on the back of the terminal block into the screw holes in the front panel to hold the SCXI-1302 securely in place.

Check the installation.

SCXI-1351 One-Slot Cable Extender

The SCXI-1351 cable extender is a miniature SCXI-1340 cable assembly. Instead of connecting to an MIO board 1 m away, the SCXI-1351 female rear connector connects to a male breakout connector that must be in the rear connector space of the slot to the left. The SCXI-1351 has a female mounting bracket connector that mates with the rear signal connector of a module, and also has a male breakout connector on the ribbon cable for connecting to a feedthrough panel or more cable extenders, or for connection to an NB5 cable for use with a DIO-96 or an AT-MIO-16D.

SCXI-1351 Installation

Follow these steps to install the SCXI-1351:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Connect the rear connector of the cable extender to the breakout connector in the adjacent slot. This attachment is similar to Step 3 in the *SCXI-1180 Installation* section, as shown in Figure E-3.
- 4. Plug the mounting bracket connector to the module rear signal connector. An alignment tab on the bracket will enter the upper board guide of the chassis.
- 5. Screw the mounting bracket to the threaded strips in the rear of the chassis.

Check the installation.

Multiple-Chassis Connections for the SCXI-1163

The SCXI-1163 can operate in a multiple-chassis system with the DIO-24, DIO-96, and the MIO boards. A multiple-chassis system can consist of up to eight SCXI-1001 chassis controlled by the same data acquisition board. Notice that you cannot use the SCXI-1000 in a multiple-chassis system. For each chassis, you need an SCXI-1350 multichassis adapter board and an NB1 ribbon cable.

Note: When connecting multiple chassis, you should use 0.5 m length ribbon cable between chassis to minimize cable length and maintain signal integrity. However, you can use a 1.0 m cable from the data acquisition board to the first chassis. When you are using the DIO-96, AT-MIO-16D, or AT-MIO-64F-5, use an NB5 ribbon cable from the data acquisition board to the first chassis, connecting positions 1 through 50 to the SCXI-1350 in the first chassis.

Installation

After you have installed the data acquisition board into the computer and the SCXI modules into each of the SCXI-1001 chassis, cable one module from each chassis to the data acquisition board as follows:

- 1. Make sure the computer and all the SCXI chassis are turned off.
- 2. Connect one end of the NB1 (or the 100-pin connector of the NB5) cable to the data acquisition board.
- 3. Plug the other end of the cable (positions 1 to 50 of the NB5 cable) into the connector with latches at the rear of the SCXI-1350 adapter board.

4. Connect another ribbon cable to the chassis extender connector in the middle of the SCXI-1350.

- 5. Plug the SCXI-1350 into the back of the SCXI module in the first chassis so that the module rear connector mates with the front connector on the SCXI-1350. When you are connecting to an SCXI-1163, be sure to set the jumpers for either a DIO-type or an MIO-type board as appropriate.
- 6. Screw the rear panel to the threaded strips in the rear of the chassis.
- 7. Connect the loose end of the ribbon cable from Step 4 into the rear connector of the second SCXI-1350 and install the adapter board.
- 8. Continue until all chassis are connected. You do not need to connect anything to the middle connector of the SCXI-1350 adapter board in the last chassis.

SCXI-1343 Rear Screw Terminal Adapter

You use the SCXI-1343 universal adapter to adapt custom wiring to the SCXI-1163. The SCXI-1343 has screw terminals and solder pads for signal connection. A strain relief is on the outside of the rear panel. Table E-6 shows the SCXI-1343 pin connections.

Table E-6. SCXI-1343 Pin Connections

| Rear Signal Connector Pin | SCXI-1163 Use | | Connection |
|------------------------------|---------------|----------|----------------|
| | Serial | Parallel | |
| 1 | No Connect | In (23) | Solder pad |
| 2 | No Connect | | Screw terminal |
| $\frac{2}{3}$ | No Connect | In (22) | Screw terminal |
| | No Connect | | Screw terminal |
| 4 5 | No Connect | In (21) | Screw terminal |
| 6 | No Connect | | Screw terminal |
| 7 | No Connect | In (20) | Screw terminal |
| 8 | No Connect | | Screw terminal |
| 9 | No Connect | In (19) | Screw terminal |
| 10 | No Connect | | Screw terminal |
| 11 | No Connect | In (18) | Screw terminal |
| 12 | No Connect | | Screw terminal |
| 13 | No Connect | In (17) | Screw terminal |
| 14 | No Connect | | Screw terminal |
| 15 | No Connect | In (16) | Screw terminal |
| 16 | No Connect | | Screw terminal |
| 17 | No Connect | In (15) | Screw terminal |
| 18 | No Connect | | Screw terminal |
| 19 | No Connect | In (14) | Screw terminal |

(continues)

Table E-6. SCXI-1343 Pin Connections (Continued)

| Rear Signal Connector Pin | SCXI-1163 Use | | Connection |
|------------------------------|-----------------|----------|------------|
| | Serial | Parallel | |
| 20 | No Connect | T (10) | Solder pad |
| 21 | No Connect | In (13) | Solder pad |
| 22 | No Connect | - (1.5) | Solder pad |
| 23 | No Connect | In (12) | Solder pad |
| 24 | DIG GND (MIO) | | Solder pad |
| 25 | No Connect | In (11) | Solder pad |
| 26 | SERDATOUT (MIO) | | Solder pad |
| 27 | DAQD*/A | In (10) | Solder pad |
| 28 | No Connect | | Solder pad |
| 29 | SLOT0SEL* | In (9) | Solder pad |
| 30 | No Connect | | Solder pad |
| 31 | SERCLK (DIO) | In (8) | Solder pad |
| 32 | No Connect | | Solder pad |
| 33 | No Connect | In (7) | Solder pad |
| 34 | No Connect | In (31) | Solder pad |
| 35 | No Connect | In (6) | Solder pad |
| 36 | No Connect | In (30) | Solder pad |
| 37 | SERCLK (MIO) | In (5) | Solder pad |
| 38 | No Connect | In (29) | Solder pad |
| 39 | No Connect | In (4) | Solder pad |
| 40 | No Connect | In (28) | Solder pad |
| 41 | No Connect | In (3) | Solder pad |
| 42 | No Connect | In (27) | Solder pad |
| 43 | No Connect | In (2) | Solder pad |
| 44 | No Connect | In (26) | Solder pad |
| 45 | No Connect | In (1) | Solder pad |
| 46 | No Connect | In (25) | Solder pad |
| 47 | SERDATOUT (DIO) | In (0) | Solder pad |
| 48 | No Connect | In (24) | Solder pad |
| 49 | No Connect | () | Solder pad |
| 50 | DIG GND (DIO) | DIG GND | Solder pad |

SCXI-1343 Installation

- 1. Insert each wire through the adapter strain relief.
- 2. Make all solder connections first.
- 3. Tighten the strain relief screws to secure the wires.
- 4. Plug the adapter board front connector into the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.

Appendix F Customer Communication

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|--|----------|
| Company | |
| Address | |
| - | |
| Fax ()Phone () | |
| Computer brand Model P | rocessor |
| Operating system | |
| SpeedMHz RAMM Display | adapter |
| Mouseyesno Other adapters installed _ | |
| Hard disk capacityM Brand | |
| Instruments used | |
| National Instruments hardware product model Revision | |
| Configuration | |
| | |
| Configuration | |
| The problem is | |
| | |
| | |
| | |
| | |
| List any error messages | |
| | |
| | |
| | |
| | |
| The following steps will reproduce the problem | |
| The following steps will reproduce the problem | |
| | |

SCXI-1163 Hardware Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

| • | SCXI-1163 Revision | | |
|-----|--|--|-----------------|
| | | | |
| • | Chassis Slot | | |
| • | Chassis Type | | |
| | | | |
| | | My Setting | Factory Setting |
| • | Jumper W2 | D | D M |
| • | Jumper W3 | D | D M |
| • | Jumper W4 | . B . A | B A |
| • | Jumper W5 | OE OE DE | OH DIO PAR |
| • | Jumper W6 | S • • • | S L P |
| Not | e: Mark your jumper positions on the jur | nner diagrams in the left column | |
| | | mper singrams in the fore condition. | |
| • | Other Modules and Chassis in System | | |
| | _ | | |
| | | | |
| • | Data Acquisition Boards Installed | | |
| | | | |

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Glossary

| Prefix | Meaning | Value |
|--------|---------|---------------------------------------|
| p- | pico- | 10-12 |
| n- | nano- | 10 ⁻¹² 10 ⁻⁹ |
| μ- | micro- | 10 ⁻⁶ |
| m- | milli- | 10-3 |
| k- | kilo- | 10^{3} |
| M- | mega- | 10 ⁶ |

degrees ohms

+5 VDC Source +5 V (signal)

A amperes

ACalternating current A/D analog-to-digital

amperes, root mean square Arms **AWG** American Wire Gauge

Celsius

CHSGND Chassis Ground counts per second cps D/A digital-to-analog D*/A Data/Address

DAQD*/A Data Acquisition Board Data/Address Line

dB decibels DC direct current DIG GND Digital Ground

Deutsche Industrie Norme DIN

DIO digital I/O

ESD electrostatic discharge **FIFO** first-in-first-out

ground **GND** hexadecimal hex

Hz hertz

I/O input/output ID identification

input current leakage I_{I}

input current I_{in} INTR* Interrupt output current I_{out} **LSB** least significant bit megabytes of memory M

meters m

multifunction I/O MIO **MISO** Master-In-Slave-Out Master-Out-Slave-In **MOSI**

Glossary

MSB most significant bit RAM random-access memory

RESET* Reset

rms root mean square

RTSI Real-Time System Integration

SCXI Signal Conditioning eXtensions for Instrumentation (bus)

SDK Software Developer's Kit

sec seconds
SERCLK Serial Clock
SERDATIN Serial Data In
SERDATOUT Serial Data Out
SLOT0SEL* Slot 0 Select

SPI Serial Peripheral Interface SPICLK Serial Peripheral Interface Clock

SS* Slot Select

UL Underwriters Laboratory

V volts

V+ Positive Supply

 $\begin{array}{ccc} VAC & volts \ alternating \ current \\ Vcc & +5 \ V \ power \ supply \\ VDC & volts \ direct \ current \\ VI & virtual \ instrument \\ V_{IH} & volts \ input \ high \\ V_{IL} & volts \ input \ low \\ \end{array}$

V_{in} volts in

 V_{OH} volts output high V_{OL} volts output low

V_{out} volts out

Vrms volts, root mean square

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